M. Tech. (Computer Science) Dissertation Series

STUDIES IN SHORT CIRCUIT FAULT DIAGNOSIS OF MULTISTAGE INTERCONNECTION NETWORKS.

a dissertation submitted in partial fulfilment of the requirements for the M. Tech. (Computer Science) degree of the Indian Statistical Institute

By

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ABSTRACT

The problem of diagnosing a single short circuit fault jointly with single switching element fault in baseline network has been studied in this work. The fault model has been described and upper bound result on the number of test vectors neccessary to detect short circuit fault in baseline network is obtained. The test vectors for detecting the fault are also determined. The diagnostic procedures for the cases of two-links short circuit case and three link short circuit case considered jointly with single switching element fault are developed. The difficulties in diagnosing the short circuit fault for higher number of links are finally discussed.

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Chapter 1
INTRODUCTION

1.1 Introduction to Multistage Interconnection Networks

To improve computational power and computing speed, the concept of Parallel Processing has become quite popular. Aided by advances in VLSI technology, multiple processor systems are configured to provide computational parallelism. Each processor is called a Processing Element (PE), which can be as complex as a fully functional contemporary microprocessor or as simple as a basic ALU block. A multiprocessor system generally consists of more than one memory modules (MM) to make processor and memory bandwidths compatible. Unlike a simple PE-MM interconnection bus in uniprocessor systems, multiprocessor systems usually have complex PE-MM data paths.

Multiprocessor systems may be designed either in *unshared memory configuration* or *shared memory configuration*. In the former, each PE has its individual MM connected as a uniprocessor system bus and exchange of data/information among PEs takes place via communication links interconnecting the PEs. In the later, any PE can acess any MM and exchange of data/information is done via predetermined memory locations. Unshared memory configuration is suitable for computations that are highly individualistic and require little data flow amongst the PEs, for example matrix transpose and multiplication operations, while the shared memory configuration is suitable for computations that are highly dependent, requiring heavy interprocessor dataflow, for example FFT computations.

Unshared memory systems are usually configured using static (dedicated) communication links among the PEs so that the interconnection network has a distinct topology. Linear array, ring, mesh, star, systolic array, hypertree, hypercube, barrell shifter, cube-conected cycles are some of the popular static interconnection topologies, some of which

are shown in Fig. 1.

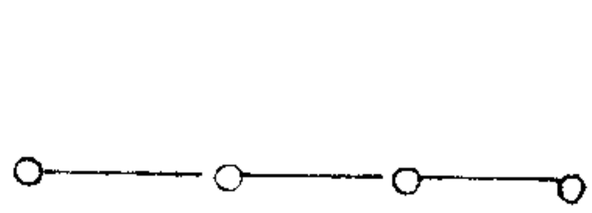
Since shared memory systems require that any PE be able to acess any MM, the PE-MM data paths need to be dynamic and memory contention should also be prevented. This is achieved by a Multistage Interconnection Network (MIN) which has programmable datapaths so that a path can be dynamically established between a pair of input-output lines. The dynamism of datapaths is achieved by using programmable solid state switching elements (SE) grouped together in one or more stages. The SEs of consecutive stages are interconnected by communication links, the topology of which give rise to MIN configurations such as benes, baseline, butterfly, omega, flip, data manipulator and indirect hypercube networks, some of which are shown in Fig.2.

1.2 Properties and Classification of MINs

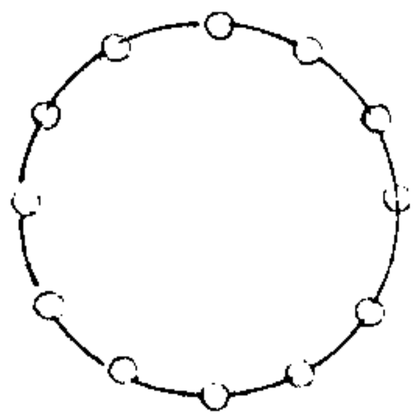
The number of stages interstage connection topolgy and switching capability of the SEs characterize a MIN. A switching element can, in general, have m input lines and n output lines, so that it is not incorrect to identify a SE as a interconnection network itself. The simplest SE is a 2x2 switch having four possible input-output routings as shown in Fig.3. Most MINs use 2x2 switching elements and restrict their valid states to straight (S-mode) and cross (X-mode) only.

The MIN can be thought of as a permutation function, which permutes the input lines to a given order at the output. In this respect, it is important to note that not all MINs are capable of providing all possible (=N!, where N is the number of input/output lines) permutations. On this basis the MINs can be classified as follows :

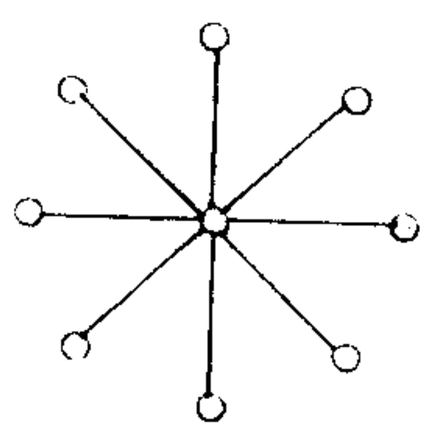
(i) Blocking or Nonrearrangeable type : These MINs cannot provide all permutations. This happens because, there is generally a unique path between a given input-output pair in the network and it blocks certain other input-output paths from being established. This class includes the baseline, omega, reverse baseline, flip and indirect hypercube



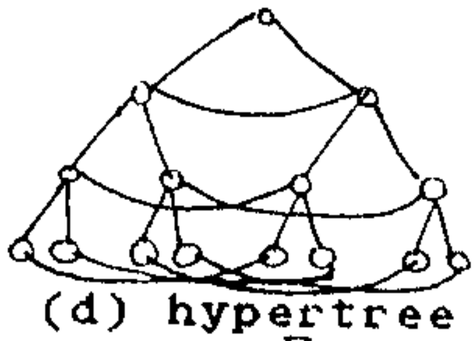
(a) linear array



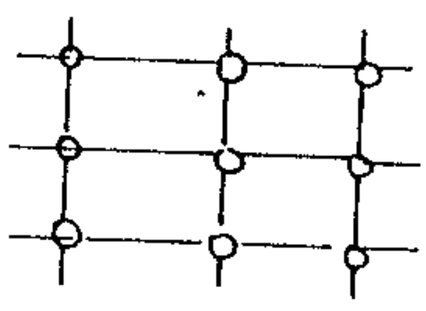
(b) ring



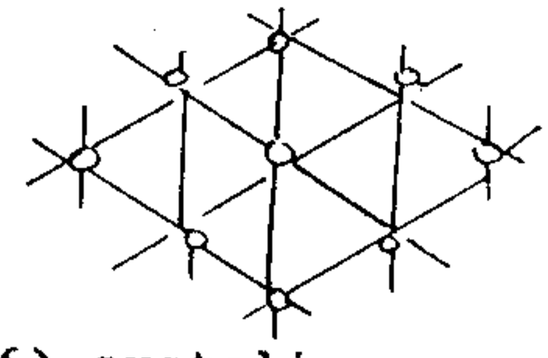
(c) star



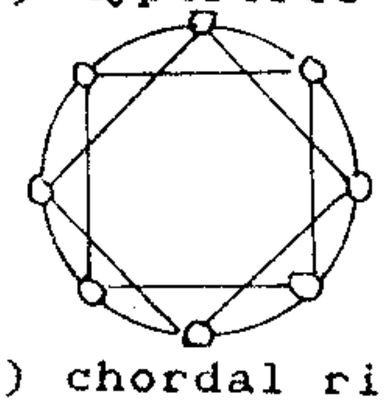
(d) hypertree



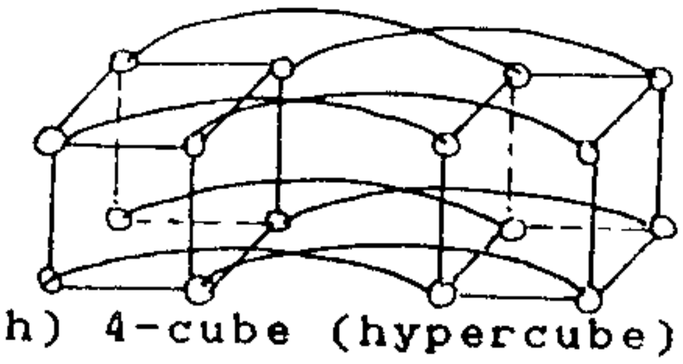
(e) mesh



(f) systolic array

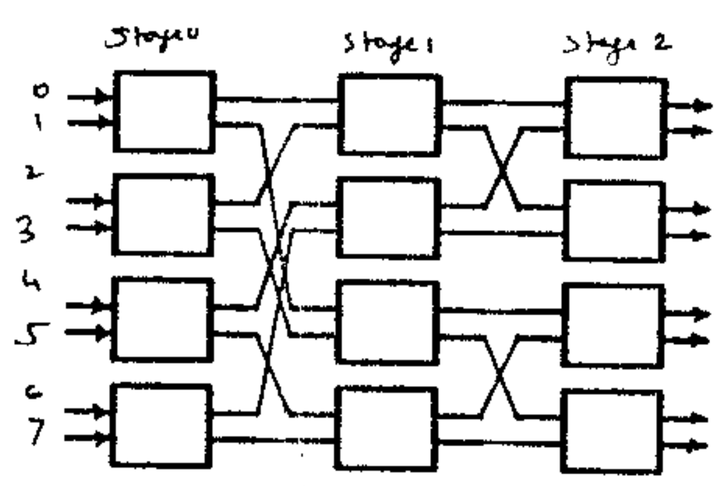


(g) chordal ring

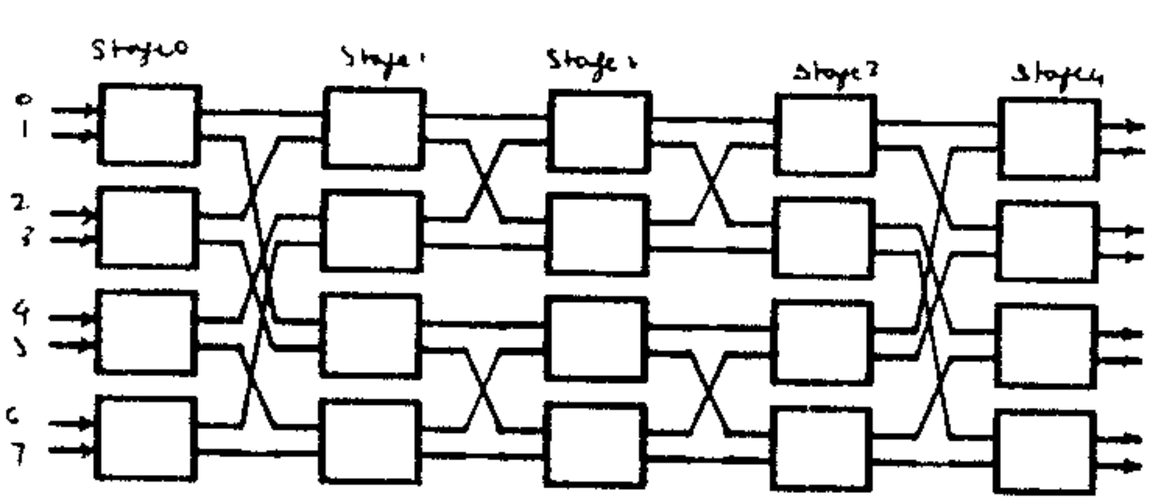


(h) 4-cube (hypercube)

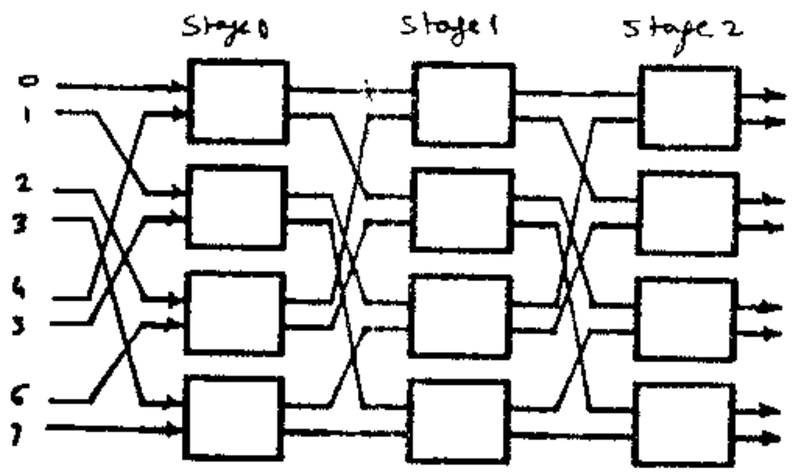
Fig.1. Static interconnection network topologies.



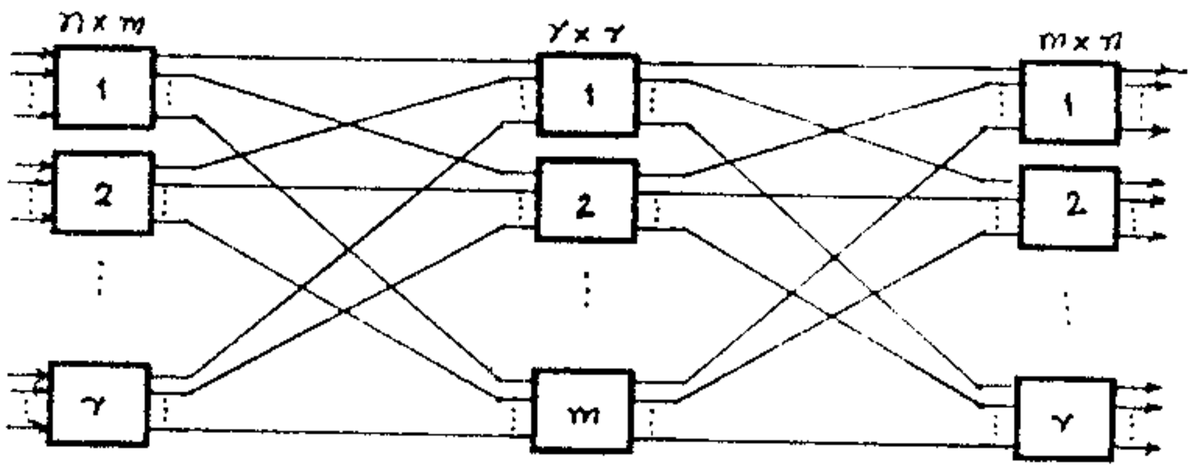
(a) baseline network



(b) Benes network



(c) omega network



(d) Clos network

Fig.2 Multistage interconnection networks

networks. Fig.4. shows instances of blocking in baseline and indirect hypercube network.

(ii) Loosely nonblocking or Rearrangeable type :

These MINs can provide all permutations of the input lines. However it may be necessary to establish an alternate path for an existing one, so as to accomodate the path for some other pair. This is called rearranging the network to achieve the required permutation. This class includes the Benes, $(3\log_2 N-4)$ stage omega network, $(2\log_2 N-1)$ stage $omega^{r}$-$omega^{-1}$ networks. Fig.5 shows instances of rearranging in a 8x8 Benes network.

(iii) Strictly nonblocking type :

These MINs have multiple paths for any input-output pair and it is always possible to establish a path independent of existing paths. The Clos network is an example of this class.

1.3 Scope of the Work

The area of fault diagnosis of MINs is assuming more and more importance because with the use of parallel systems expanding rapidly, system reliability measures are becoming prominent parameters for system performance.

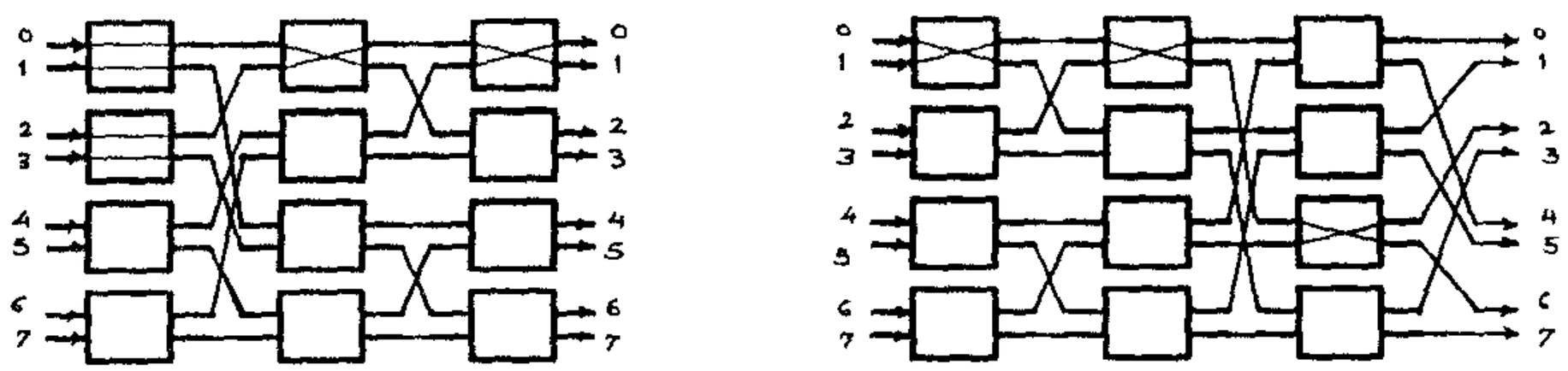
The problem of diagnosing a single short circuit fault jointly with single SE fault in baseline network has been studied in this work. The fault model has been described and upper bound result on the number of test vectors neccessary to detect short circuit fault in baseline network is obtained. The test vectors for detecting the fault are also determined. The diagnostic procedures for the cases of two-links short circuit case and three link short circuit case considered jointly with single SE fault are developed. The difficulties in diagnosing the short circuit fault for higher number of links are discussed.

1.4 Organization of the report

The current state of work in the fault diagnosis related to MINs is revived in chapter 2. The study of single SE fault diagnosis is summarised in more detail in section 2.2 because

(a) (b) (c) (d)

Fig.3 A 2x2 switching element. (a)straight connection (S-mode). (b)cross connection (X-mode). (c)lower broadcast (LB-mode). (d)Upper broadcast (UB-mode).



(a) baseline (b) indirect 3-cube

Fig.4 Blocking networks

(a) The path 2-1 blocks paths 3-0, 0-1, 7-1 etc.

(b) The path 1-6 blocks paths 0-4, 0-6, 0-2 etc.

(a)

(b)

Fig.5 Rearrangeable network (Benes)

(a) Paths 2-6 and 1-0 block the path 3-1.

(b) Paths 2-6, 1-0, 3-1 are established after rearrangement.

we wish to develop fault diagnosis procedures for short circuit faults jointly with the single SE fault.

Chapter 3 discusses the bulk of work done. In this, the fault model is first defined in terms of the output response behaviour of these faults. The upper bound results for fault detection are determined in section 3.2. In section 3.4, we discuss the fault diagnosis of two-link short circuit fault. The three-link short circuit fault is discussed in section 3.5. In section 3.6 the short circuit fault diagnosis of Benes network is proposed.

Chapter 2

REVIEW OF FAULT DIAGNOSIS OF MINs

2.1 Literature Survey

Study of fault diagnosis of MINs was initiated in the early 70's by Opferman et. al.in [OT71] in which, they gave a diagnostic procedure for Benes network considering a restricted fault model with only two faulty states of the SEs. They developed a test set generation procedure using a looping algorithm.

[A82] is a survey of the fault diagnosis works related to blocking networks, rearrangeable networks and fault tolerant design of MINs.

Feng et. al. give a very comprehensive fault diagnosis procedure for single fault of a baseline network in [FW81]. They describe a general fault model of the SE and the diagnosis is done by observations on the output side only. Testing consists of two phases in which all the SEs are set in S-mode and X-mode and there are two tests in each phase. A fault can be detected in four tests independent of network size. Single fault diagnosis requires at most max(12, $6+2\lceil\log_2(\log_2 N)\rceil$) tests for an NxN baseline network. Certain SE faults cannot be accurately located and such faults are also indistinguishable from link stuck-type fault. This is because these faults exhibit exactly same output response for any test input and any setting of the baseline network.

[FY86] design test procedures for fault diagnosis of rearrangeable networks. Unlike [OT71], instead of a Benes network, they use a $(2\log_2 N-1)$ stage $\text{omega}^r\text{-omega}^{-1}$ network which is equivalent to a Benes network as shown in [L81].

[FZ91] gives fault diagnosis procedure for blocking MINs having four valid states of the SEs. They have again used a baseline network for study, since most other blocking networks are equivalent to a baseline network as demonstrated in [WF80].

2.2 Single Fault Diagnosis of a Baseline Network ([FW81])

As discussed in section 1.3, our aim is to provide diagnostic procedures for short circuit faults, so as to make the test procedure of a baseline network *complete*. Since we shall be refering to the [FW81] work frequently in chapter 3, we feel it appropriate to discuss the relevant portions vis-a-vis short circuit faults here. This will also help to introduce the terminology to be used further on.

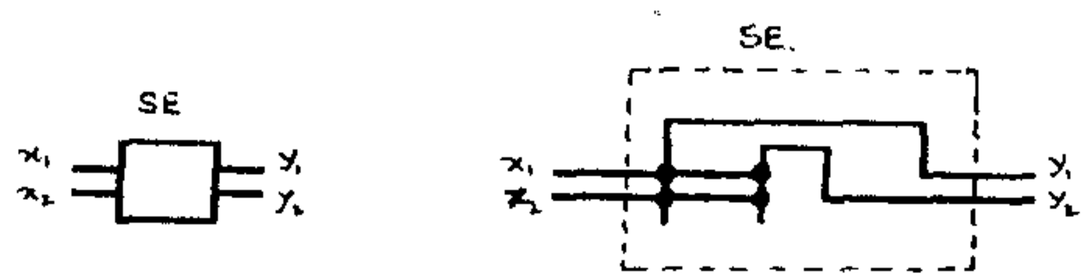
2.2.1 Fault Model and Test Set for Testing a SE/link

A fault located at a link can be modelled by a link stuck-at-0 (s-a-0) or stuck-at-1 (s-a-1). A 2x2 SE can be modelled by a 2x2 crosspoint switching matrix as shown in Fig.6. An SE in this model can have 16 possible states, which covers all the possible input-output connections of a 2x2 switch. Hence this model is the most general model of a 2x2 SE. Table I shows the set $S = (S_0, \ldots, S_{15})$ of 16 states and the encoding of these states.

Definition 1 : The states of an SE which are *allowed* in a MIN are called the *valid states* of the SE for that MIN. The remaining states of S form the set of *faulty states*.

Most of the MINs, for example baseline, flip, Benes and indirect hypercube, have S_5 and S_{10} as the valid states. Some MINs, for example omega and regular SW banyan networks, also include S_3 and S_{12} as valid states.

For an SE with n valid states, there are $(16)^n$ different state configurations in which it can behave. The set of **ordered n-tuples** : $((s_1, s_2, \ldots, s_n) \mid s_i \in S,\ 1 \le i \le n)$ gives all the configurations of the SE. Among the $(16)^n$ configurations only one is fault-free, the rest represent a fault of the SE. Thus the number of faulty configurations in this general fault model increases exponentially with the number of valid states. In a baseline network, therefore, we have one fault-free configuration and 255 faulty configurations. Except four faults, all are diagnosable by observing output responses of various tests. To design a test set for switching element and link stuck-type faults, the

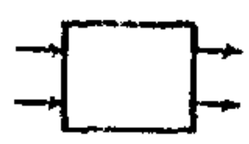
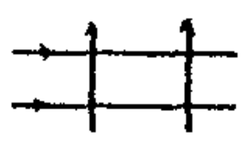
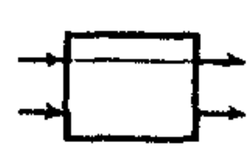
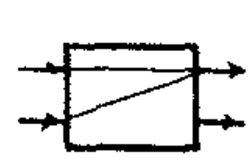
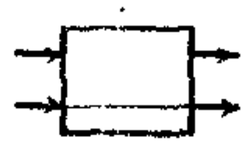
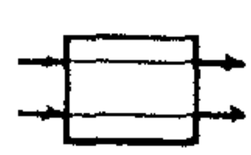
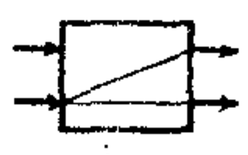
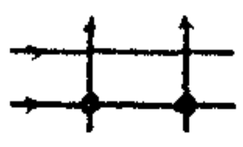
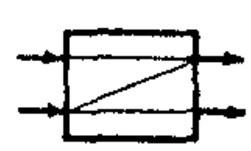
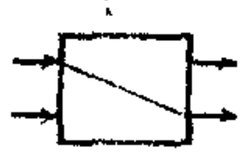
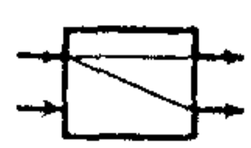
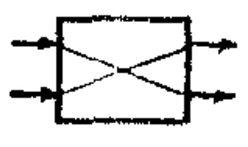
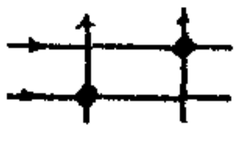
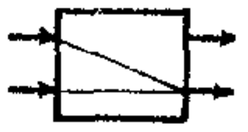
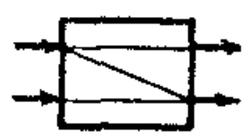
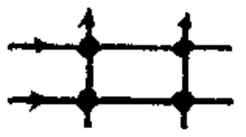


(a) (b)

Fig. 6.(a)switching element (SE). (b) 2x2 crosspoint switching matrix (CSM)

Table I

Set of 16 states of a 2x2 SE and their encoding

state	SE symbol	CSM symbol	state	SE symbol	CSM symbol
S_0			S_8		
S_1			S_9		
S_2			S_{10}		
S_3			S_{11}		
S_4			S_{12}		
S_5			S_{13}		
S_6			S_{14}		
S_7			S_{15}		

test bits which cause observable faulty outputs must be determined. Table II and table III indicate the necessary test inputs.

Definition 2 : A logically unidentified value is denoted by – and a logically erroneous value by Φ.

The binary logic value of a open circuited link is represented by –. The binary logic value of a short circuited link is represented by Φ. Note that a shorted condition is observed only if the shorted pair of links receive complementary test bits, otherwise the fault is transparent.

The values – and Φ depend on the circuit implementation of the MIN, however an arbitrary but consistent assignment of 0 or 1 will not affect the fault diagnosis. In fact there is an algorithm to accurately distinguish between these types of faults.

From tables II and III it can be observed that only two test inputs $(x_1, x_2) = (0, 1)$ and $(x_1, x_2) = (1, 0)$ are needed to observe the SE/link faults. The test set should therefore ensure that the SEs and the links are tested with complementary test bits.

2.2.2 Test Vector Design and Algorithm for Single Fault Diagnosis.

Definition 3 : Links are assigned addresses by identifying them with the stage, the input side of which they are connected to and numbering them from top to bottom. The stages of the MIN are numbered from left to right starting from 0, and if n is the number of stages in the MIN, the output side links are designated as links of stage n. A Link is called *even* if its binary address contains even number of 1's, *odd* otherwise.

Accordingly, in an NxN MIN with $N=2^n$ and t-stages, a link of the j^{th} stage will be identified as $P_j=(p_{n-1}\ldots p_1 p_0)_j$, $0 \le j \le n$. Fig.7 shows the addressing scheme for a 16x16 baseline network. A path of the MIN will be given as a (n+1)-tuple $P = (P_0, P_1, \ldots, P_{n-1}, P_n)$ of its links or by anyone of its links, say P_i, if the MIN setting is known.

TABLE II

FAULTS, TEST INPUTS, AND OUTPUTS IN VALID STATE S_{10}

	Fault	Test x_1	Test x_2	Output Normal $\hat{x}_1$	Output Normal $\hat{x}_2$	Output Faulty $\hat{x}_1$	Output Faulty $\hat{x}_2$
Part I: Link Stuck Fault	$x_1^*, \bar{x}_1^*$	1	0	1	0	0	0
		1	1	1	1	0	1
	$x_1^!, \bar{x}_1^!$	0	0	0	0	1	0
		0	1	0	1	1	1
	$x_2^*, \bar{x}_2^*$	0	1	0	1	0	0
		1	1	1	1	1	0
	$x_2^!, \bar{x}_2^!$	0	0	0	0	0	1
		1	0	1	0	1	1
Part II: Switching Element Fault	S_{10}-S_0	0	1	0	1	-	-
		1	0	1	0	-	-
		0	0	0	0	-	-
		1	1	1	1	-	-
	S_{10}-S_1	0	1	0	1	1	-
		1	0	1	0	0	-
		0	0	0	0	0	-
		1	1	1	1	1	-
	S_{10}-S_2	0	1	0	1	-	1
		1	0	1	0	-	0
		0	0	0	0	-	0
		1	1	1	1	-	1
	S_{10}-S_3	0	1	0	1	1	1
		1	0	1	0	0	0
	S_{10}-S_4	0	1	0	1	-	0
		1	0	1	0	-	1
		0	0	0	0	-	0
		1	1	1	1	-	1
	S_{10}-S_5	0	1	0	1	1	0
		1	0	1	0	0	1
	S_{10}-S_6	0	1	0	1	-	◊
		1	0	1	0	-	◊
		0	0	0	0	-	0
		1	1	1	1	-	1
	S_{10}-S_7	0	1	0	1	1	◊
		1	0	1	0	0	◊
	S_{10}-S_8	0	1	0	1	0	-
		1	0	1	0	1	-
		0	0	0	0	0	-
		1	1	1	1	1	-
	S_{10}-S_9	0	1	0	1	◊	-
		1	0	1	0	◊	-
		0	0	0	0	0	-
		1	1	1	1	1	-
	S_{10}-S_{11}	0	1	0	1	◊	1
		1	0	1	0	◊	0
	S_{10}-S_{12}	0	1	0	1	0	0
		1	0	1	0	1	-
	S_{10}-S_{13}	0	1	0	1	◊	0
		1	0	1	0	◊	1
	S_{10}-S_{14}	0	1	0	1	0	◊
		1	0	1	0	1	◊
	S_{10}-S_{15}	0	1	0	1	◊	◊
		1	0	1	0	◊	◊

TABLE III

FAULTS, TEST INPUTS, AND OUTPUTS IN VALID STATE S_5

	Fault	Test x_1	Test x_2	Output Normal $\hat{x}_1$	Output Normal $\hat{x}_2$	Output Faulty $\hat{x}_1$	Output Faulty $\hat{x}_2$
Part I: Link Stuck Fault	$x_1^*, \bar{x}_2^*$	1	0	0	1	0	0
		1	1	1	1	1	0
	$x_1^!, \bar{x}_2^!$	0	0	0	0	0	1
		0	1	1	0	1	1
	$x_2^*, \bar{x}_1^*$	0	1	1	0	0	0
		1	1	1	1	0	1
	$x_2^!, \bar{x}_1^!$	0	0	0	0	1	0
		1	0	0	1	1	1
Part II: Switching Element Fault	S_5-S_0	0	1	1	0	-	-
		1	0	0	1	-	-
		0	0	0	0	-	-
		1	1	1	1	-	-
	S_5-S_1	0	1	1	0	1	-
		1	0	0	1	0	-
		0	0	0	0	0	-
		1	1	1	1	1	-
	S_5-S_2	0	1	1	0	-	1
		1	0	0	1	-	0
		0	0	0	0	-	0
		1	1	1	1	-	1
	S_5-S_3	0	1	1	0	1	1
		1	0	0	1	0	0
	S_5-S_4	0	1	1	0	-	0
		1	0	0	1	-	1
		0	0	0	0	-	0
		1	1	1	1	-	1
	S_5-S_6	0	1	1	0	-	◊
		1	0	0	1	-	◊
		0	0	0	0	-	0
		1	1	1	1	-	1
	S_5-S_7	0	1	1	0	1	◊
		1	0	0	1	0	◊
	S_5-S_8	0	1	1	0	0	-
		1	0	0	1	1	-
		0	0	0	0	0	-
		1	1	1	1	1	-
	S_5-S_9	0	1	1	0	◊	-
		1	0	0	1	◊	-
		0	0	0	0	0	-
		1	1	1	1	1	-
	S_5-S_{10}	0	1	1	0	0	1
		1	0	0	1	1	0
	S_5-S_{11}	0	1	1	0	◊	1
		1	0	0	1	◊	0
	S_5-S_{12}	0	1	1	0	0	0
		1	0	0	1	1	1
	S_5-S_{13}	0	1	1	0	◊	0
		1	0	0	1	◊	1
	S_5-S_{14}	0	1	1	0	0	◊
		1	0	0	1	1	◊
	S_5-S_{15}	0	1	1	0	◊	◊
		1	0	0	1	◊	◊

Algorithm A : Test vector design

1. Even links of stage) receive test bit 1, odd links receive test bit 0.

end.

Definition 4 : The *S-phase* of testing consists of setting all the SEs in the S-mode and performing the following tests :

(i) feed the test vector, observe the output responses

(ii) feed the *complementary* test vector, observe the output responses.

The *X-phase* of testing is done exactly as above with all the SEs set in X-mode.

Algorithm B : Testing a baseline network for single faults.

1. Generate the test vector by algorithm A.
2. Using the test vector of step 1 perform the S-phase test.
3. Using the test vector of step 1 perform the X-phase test.
4. If there exists a single fault in the network some faulty response lines will be observed. As discussed in sec.2.2.3, the fault can be diagnosed by additional tests if necessary.

end.

Theorem 1 : The algorithm B ensures that all links and SEs receive complementary test bits in both valid states.

Proof : By testing the network in S-phase and X-phase, the SEs are tested in both valid states. Since each phase involves tests with complementary test vectors, every link receives complementary test bits. It remains to be shown that the SEs receive complementary test inputs in both phases.

(i) S-phase

Consider an NxN baseline, $N = 2^n$. In the S-phase a path P containing the link $(p_{i-1}\ldots p_0)_o$ will contain the link $(p_0\ldots p_{i-1}p_{n-1}\ldots p_i)_i$, $0\leq i\leq n$.

Now the input links of any SE of stage i, $0\leq i\leq n-1$, will be of the form $P_1=(p_0\ldots p_{i-1}p_{n-1}\ldots p_i)_i$ and $P_2=(p_0\ldots p_{i-1}p_{n-1}\ldots \overline{p_i})_i$, which will receive the same test

bits as the links $P_3=(p_{n-1}\cdots p_{i+1}p_i p_{i-1}\cdots p_0)_o$ and $P_4=(p_{n-1}\cdots p_{i+1}\overline{p}_i p_{i-1}\cdots p_0)_o$ respectively. P_1, P_3 have the same number of 1's and so do P_2, P_4. Since P_1, P_2 form an even-odd pair P_3, P_4 also form an even-odd pair. Hence by algorithm A, P_1, P_2 receive complementary test bits in S-phase.

(ii) X-phase

In the X-phase a path P containing the link $(p_{n-1}\cdots p_0)_o$ will contain the link $(\overline{p}_0\cdots\overline{p}_{i-1}p_{n-1}\cdots p_i)_i$, $0\le i\le n$.

Now the input links of any SE of stage i, $0\le i\le n-1$, will be of the form $P_1=(\overline{p}_0\cdots\overline{p}_{i-1}p_{n-1}\cdots p_i)_i$ and $P_2=(\overline{p}_0\cdots\overline{p}_{i-1}p_{n-1}\cdots\overline{p}_i)_i$, which will receive the same test bits as the links $P_3=(p_{n-1}\cdots p_i p_{i-1}\cdots p_0)_o$ and $P_4=(p_{n-1}\cdots\overline{p}_i p_{i-1}\cdots p_0)_o$ respectively.

Case a : i is even :

P_1, P_3 form an even-odd pair and so do P_2, P_4. Since P_1, P_2 are an even-odd pair P_3, P_4 are also an even-odd pair.

Case b : i is odd :

P_1, P_3 form either an even-even or an odd-odd pair and so do P_2, P_4. Since P_1, P_2 are an even-odd pair P_3, P_4 are also an even-odd pair.

Thus by algorithm A, P_1, P_2 will receive complementary test bits in X-phase.

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Fig.8 and Fig.9 show that all SEs receive complementary test inputs in both phases in a baseline network.

From tables I, II and theorem 1, it can be concluded that four test are necessary and sufficient to detect single fault at the SE or link level, independent of the network size.

Definition 6 : Define the faulty output response as *unary* if the observed response is 00 or 11 in the two tests of a phase. Define it as *binary* if the observed response is 01 or 10, vis-a-vis a normal response of 10 or 01 respectively, in the two tests of a phase.

Note that open and short circuit faults will show unary response. Example of unary and binary faults is shown in

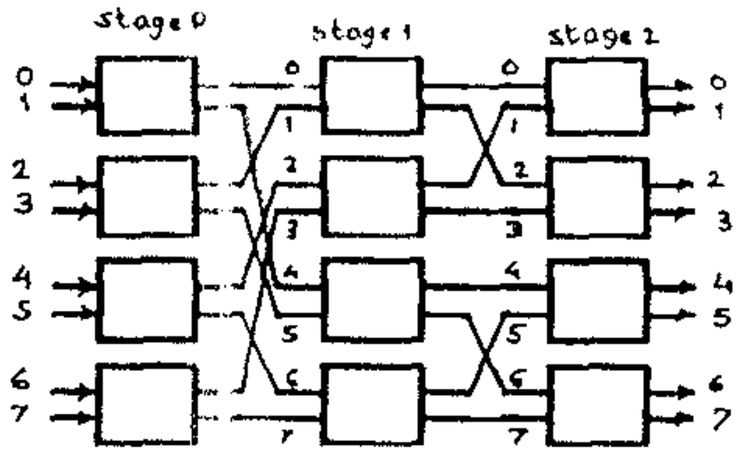

Fig.7 Address assignment to links in a 8x8 baseline

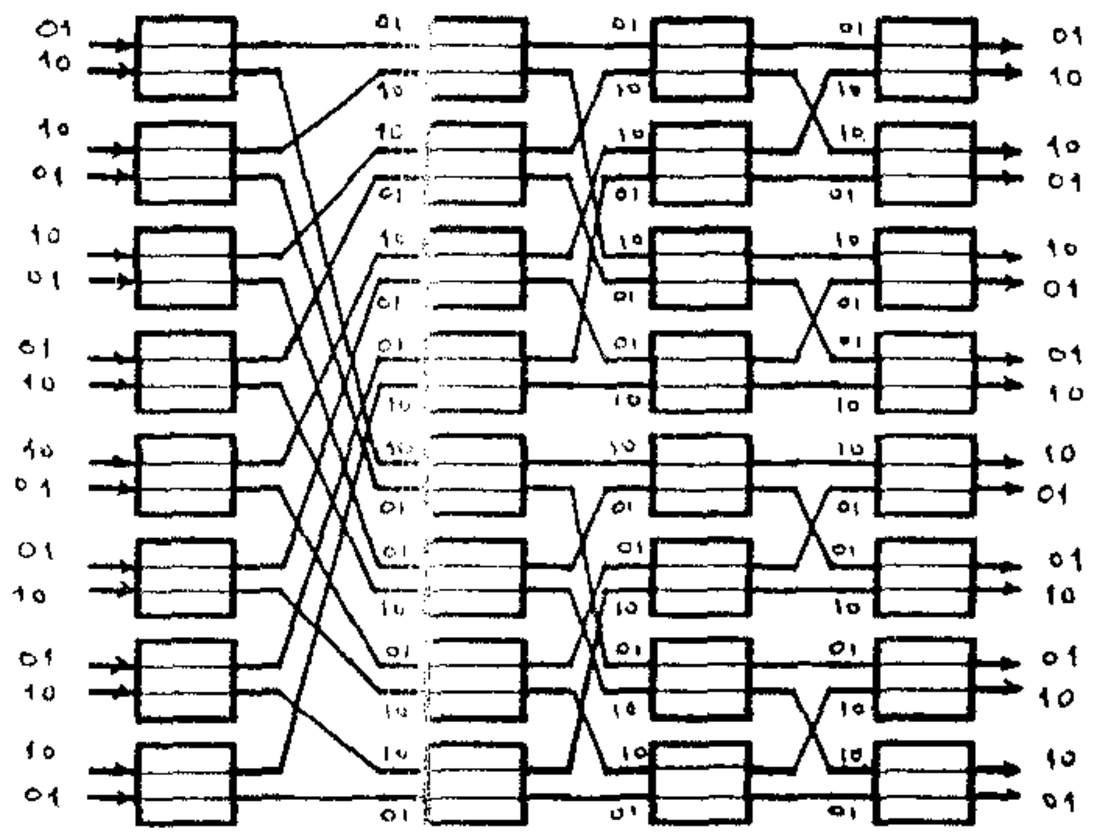

Fig.8 Fault free response of a baseline network to the tests in S-phase

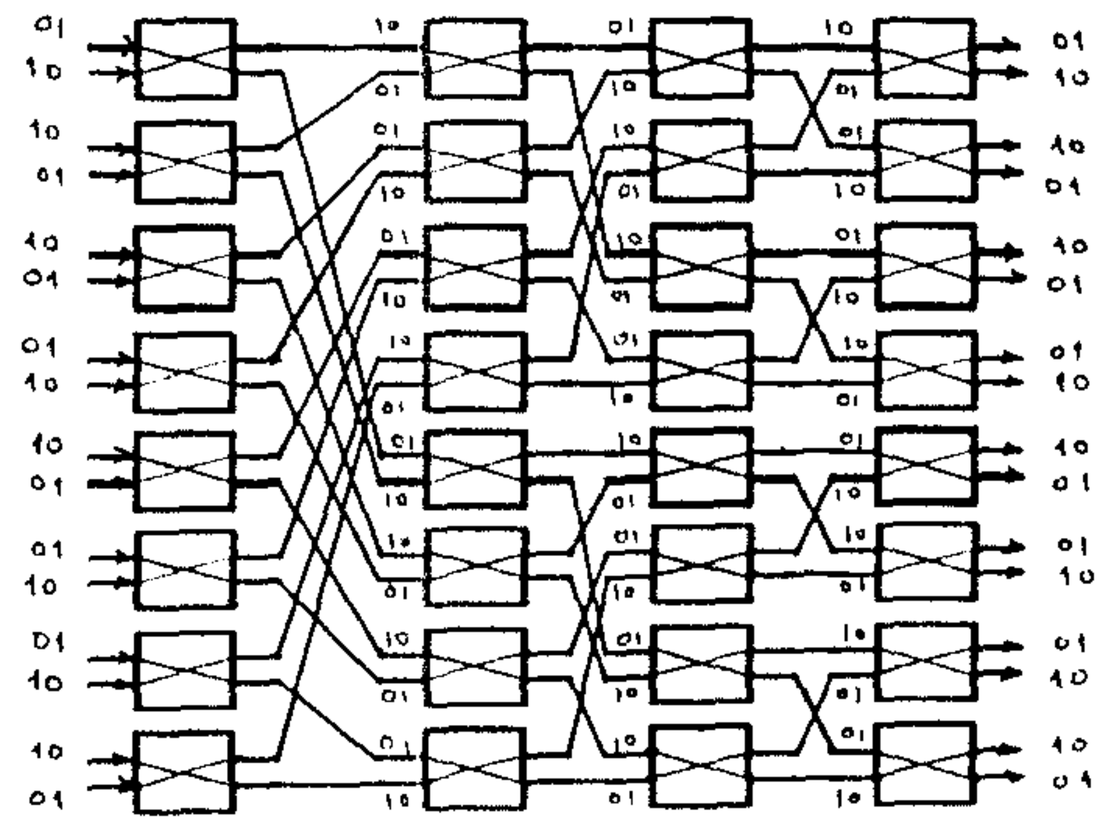

Fig.9 Fault free response of a baseline network to the tests in X-phase

fig.10.

Algorithm C : Resolve short and open circuit condition of unary response fault

// It is necessary to know the location of the faulty SE. //

1. set the network as in the phase in which the unary fault was observed.
2. Identify the input lines which lead to the faulty SE. Test the SE with test inputs (0, 0) and (1, 1) on these input lines and observe the faulty output lines. If the response is binary then fault is of short circuit type, else it is of the open circuit type.

end.

2.2.3 Casewise Diagnosis of Single Fault

The four tests of algorithm B detect the fault and the following data is available from these tests : the number of faulty output lines, the behaviour of the faulty lines, and the phase in which they were observed. This data and a few other tests are sufficient to diagnose the fault. The 255 faults of the SE and the link stuck-type fault can be classified as follows :

1) One-response fault : There is only one faulty output which can be in S-phase or X-phase test.

2) Seperated two-response fault : There are two faulty outputs. One of them occurs in the S-phase test and the other occurs in the X-phase test.

3) Nonseperated two-response fault : There are two faulty outputs both occur either in the S-phase or the X-phase test.

4) Multiple-response fault : There are more than two faulty outputs

Fig. 12 pictorially shows the classification of all the 255 faults of the SE. Each of these four cases are considered in the following paragraphs.

Case 1 : This case cover the 12 faults in the union of the sets $(S_1, S_3, S_8, S_{11}, S_{12}, S_{14})x(S_5)$ and $(S_{10})x(S_1, S_3, S_4, S_9, S_{12}, S_{13})$. The faulty SE can be anyone of the switching

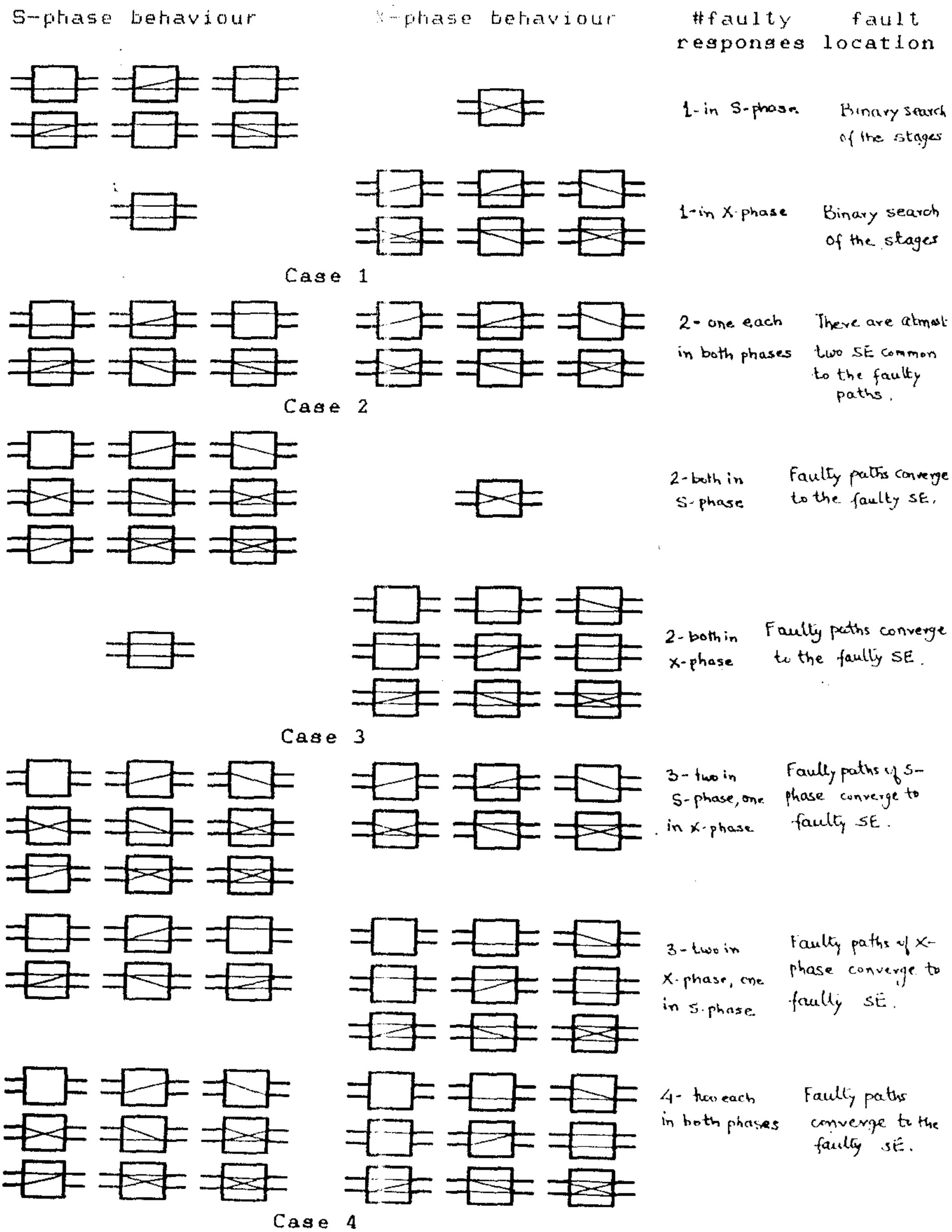

Fig 12. Classification of single SE faults.

elements lying on the faulty path and hence the data available from fault detection tests is insufficient for fault location. Using additional tests and technique of binary search of the stages, this fault can be diagnosed in at most $4+2\lceil\log_2(\log_2 N)\rceil$ tests.

Case 2 : This case covers the 36 faults in the the set $(S_2, S_3, S_8, S_{11}, S_{12}, S_{14}) \times (S_1, S_3, S_4, S_7, S_{12}, S_{13})$. It also includes the link stuck-type fault. The SE faults can be further classified as shown in tablesIV and V. In this case at most two SEs will be common to the faulty paths. Faults of subcase A,B,C,D and E can be diagnosed in at most 16 tests, independent of the network size. The ambiguity of fault location of subcase F faults cannot be resolved by any test in which only the input-output terminals of the MIN are accessible. The subcase F faults are also indistinguishable from link stuck-type faults. Fig.11 shows the one-one corresspondence between a subcase F fault and link stuck-type fault.

Case 3 : This case covers the 18 faults in the union of the sets $(S_0, S_1, S_4, S_5, S_6, S_7, S_9, S_{13}, S_{15}) \times (S_5)$ and $(S_{10}) \times (S_0, S_2, S_6, S_8, S_9, S_{10}, S_{11}, S_{14}, S_{15})$. The fault outputs converge uniquely to the faulty SE. Hence this fault can be diagnosed in at most 6 tests after resolving the short and open circuit conditions of the unary faulty outputs.

Case 4 : This case can be subdivided into the following subcases

(a) Three-response faults : This case covers the 108 faults in the union of the sets $(S_0, S_1, S_4, S_5, S_6, S_7, S_9, S_{13}, S_{15}) \times (S_1, S_3, S_4, S_7, S_{12}, S_{13})$ and $(S_2, S_3, S_8, S_{11}, S_{12}, S_{14}) \times (S_0, S_2, S_5, S_8, S_9, S_{10}, S_{11}, S_{14}, S_{15})$.

(b) Four-response faults : This case covers the 81 faults in the set $(S_0, S_1, S_4, S_5, S_6, S_7, S_9, S_{13}, S_{15}) \times (S_0, S_2, S_5, S_8, S_9, S_{10}, S_{11}, S_{14}, S_{15})$.

In both the above subcases the two faulty paths of one of the phases uniquely converge to the faulty SE. Hence this fault can be diagnosed in at most 8 tests after resolving the

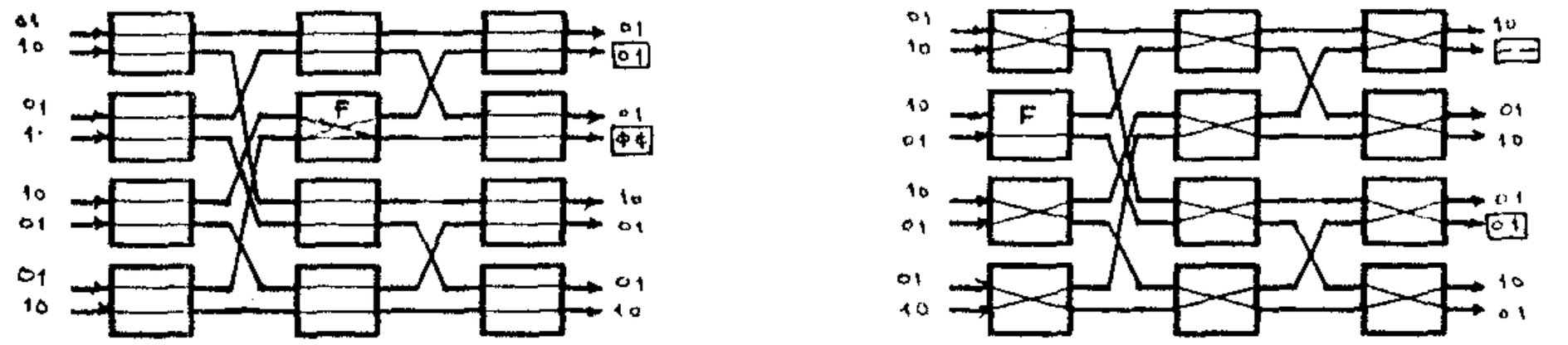

Fig.10 Examples of unary and binary behaviour of faulty output lines. F indicates faulty SE.

Table IV

Faulty output pattern for Case 2 faults.

Subcase	Faulty responses	
	one phase	other phase
A	Binary	Binary
B	Binary	Unary (ΦΦ)
C	Binary	Unary (--)
D	Unary (ΦΦ)	Unary (--)
E	Unary (ΦΦ)	Unary (ΦΦ)
F	Unary (--)	Unary (--)

Table V

Classificaton of the Case 2 faults.

Fault in state S_5	Fault in state S_{10}					
	S_9	S_{12}	S_{11}	S_{14}	S_2	S_0
S_9	A	A	B	B	C	C
S_{12}	A	A	B	B	B	C
S_7	B	B	E	E	D	D
S_{13}	B	B	E	E	D	D
S_1	C	C	C	C	F	F
S_4	C	C	C	C	F	F

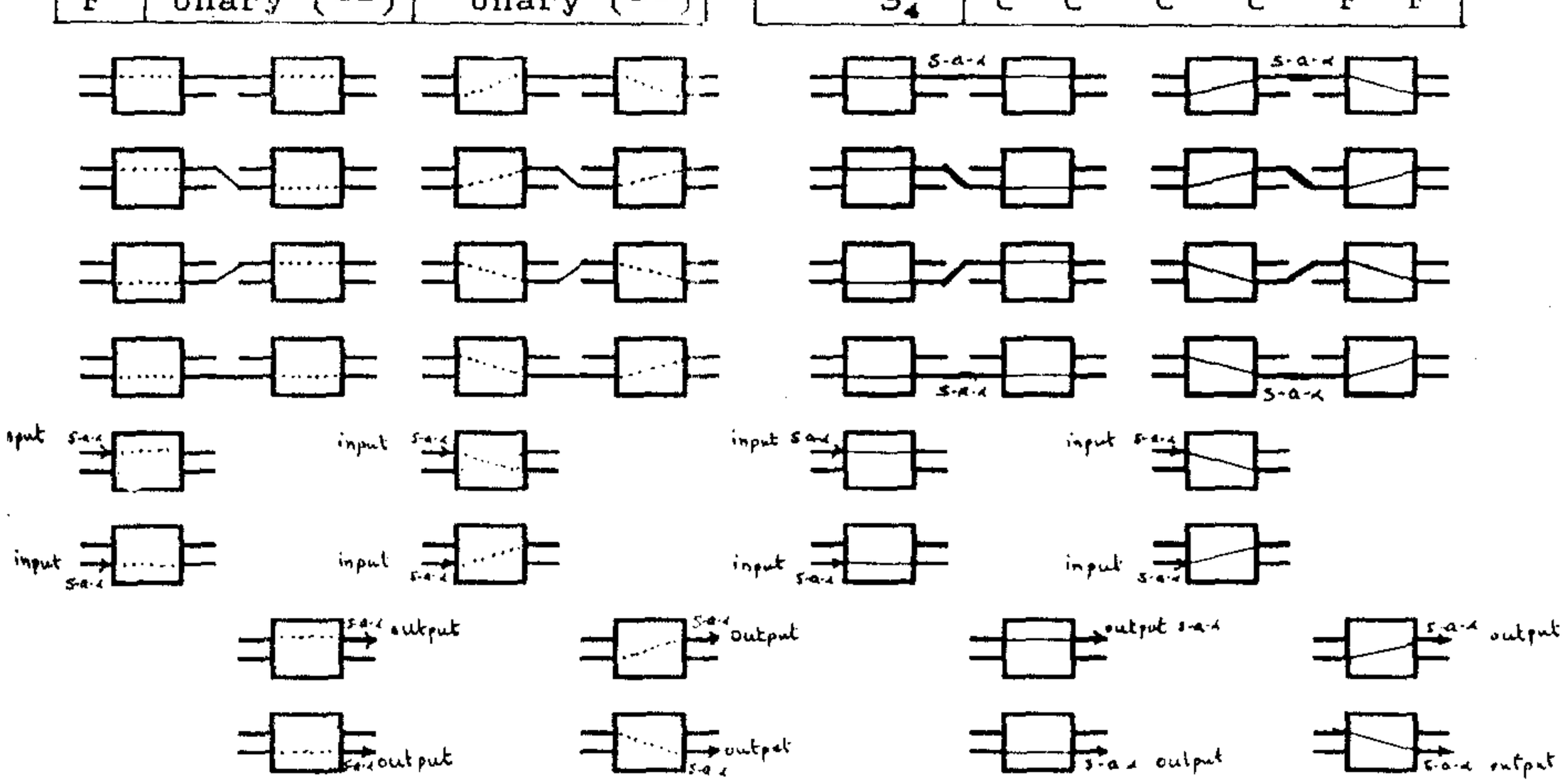

Fig.11 Behavioural equivalence of subcase F fault of SE and link stuck-type fault. (Among the pair of dotted lines, one is an open connection and other is a normal connection)

short and open circuit conditions of the unary faulty outputs.

Table VI summarises the results of single switching element fault diagnosis of the baseline network.

TABLE XII
CHARACTERISTICS OF SINGLE FAULTS

Cases		Fault Types	Faulty Output Pattern	No. of Fault Types	No. of Tests Needed For Determining the Fault Location	No. of Additional Tests For Determining the Fault Type
Case 1: One-Response Fault		$(S_3,S_5),(S_{12},S_5),(S_{10},S_3),(S_{10},S_{12})$	Table 4	4	$4+2\lceil\log_2(\log_2 N)\rceil$ or $4+2\lceil\log_2(\log_2 N)\rceil$	0
		$(S_2,S_5),(S_8,S_5),(S_{11},S_5),(S_{14},S_5),$ $(S_{10},S_1),(S_{10},S_4),(S_{10},S_7),(S_{10},S_{13})$	Table 4	8	$4+2\lceil\log_2(\log_2 N)\rceil$ or $4+2\lceil\log_2(\log_2 N)\rceil$	2
Case 2: Separated Two-Response Fault	Subcase A	$(S_{12},S_{12}),(S_{12},S_3),(S_3,S_{12}),(S_3,S_3)$	Table 8	4	4 or 8	0
	Subcase B & C	$(S_{12},S_{13}),(S_{12},S_7),(S_3,S_{13}),(S_3,S_7),$ $(S_{11},S_{12}),(S_{11},S_3),(S_{14},S_{12}),(S_{14},S_3),$ $(S_{12},S_4),(S_{12},S_1),(S_3,S_4),(S_3,S_1),$ $(S_7,S_{13}),(S_7,S_3),(S_8,S_{12}),(S_8,S_3)$	Table 9	16	4 or 8	2
	Subcase D & E	$(S_2,S_{13}),(S_2,S_7),(S_8,S_{13}),(S_8,S_7),$ $(S_{11},S_4),(S_{11},S_1),(S_{14},S_4),(S_{14},S_1),$ $(S_{11},S_{13}),(S_{11},S_7),(S_{14},S_{13}),(S_{14},S_7)$	Table 10	12	4, 8 or 12	0 or 4
	Subcase F	$(S_2,S_4),(S_2,S_1),(S_8,S_4),(S_8,S_1)$	Table 11	4	(cannot be located at the single switching element level)	(not a distinguishable from a link stuck fault)
Case 3: Non-Separated Two-Response Fault		$(S_0,S_1,S_4,S_5,S_6,S_7,S_9,S_{13},S_{15})\times(S_5)$; $(S_{10})\times(S_0,S_2,S_6,S_8,S_9,S_{10},S_{11},S_{14},S_{15})$		18	4	0 or 2
Case 4: Multiple-Response Fault		$(S_0,S_1,S_4,S_5,S_6,S_7,S_9,S_{13},S_{15})\times(S-S_5)$; $(S-S_{10})\times(S_0,S_2,S_6,S_8,S_9,S_{10},S_{11},S_{14},S_{15})$		189	4	0, 2, or 4

Chapter 3

SHORT CIRCUIT FAULT DIAGNOSIS

3.1 Problem definition and Motivation

In chapter 2 we have seen how single faults in a baseline network are diagnosed. The faults were restricted to switching element or link stuck-type fault. There is another important type of prevailent fault namely, short circuit fault among the links of the MIN. The problem is *'To study and develop diagnostic procedures for short circuit fault in MINs'*. It is desirable that these procedures also incorporate the fault diagnosis of switching element faults as well.

A little insight into the problem will reveal that this general problem has the following parameters :

1. the number of links that belong to a short circuited group,
2. the number of disjoint groups of short circuited links or in other words, whether there is a single short circuit fault or there are multiple short circuit faults,
3. restrictons on the location of the faults i.e. whether or not the short circuited links belong to the same stage and
4. the class of MIN for which the fault diagnosis is studied.

Here we have restricted the problem to single fault with the number of short circuited links limited to at most three for the baseline network only. The fault location is unrestricted. The short circuit fault diagnosis for Benes network in the above framework is also proposed.

The upper bound on the number of tests for any general MIN in which the valid states of the SEs are either S-mode or X-mode has been obtained and the corressponding test vectors are also developed.

The area of fault diagnosis of MINs is assuming more and more importance because with the use of parallel systems expanding rapidly, system reliability measures are becoming prominent parameters for system performance.

To guarantee fault-free performance it is therefore

necessary to be able to *test* system components. It is desirable that such test procedures be algorithmic in nature so that automated implementation is possible and in view of widespread LSI/VLSI implementation of most system components, such test procedures should access only the input/output terminals.

The motivation behind the study of short circuit fault of MINs is that this fault is completely absent in the existing literature. Remarkably, this fault has not assumed importance in most fault diagnosis studies inspite of the fact that short circuit between two tracks (primarily adjacent) is one of the chief causes of defects in LSI/VLSI circuits. The study of short circuit fault will truly *complete* the fault diagnosis of single fault of baseline network.

[A82] mentions about short circuit fault behaviour restricted to the input/output lines of an SE which can be modelled by an equivalent fault of the SE. But a short circuit among adjacent tracks may, depending on the VLSI layout, translate to a logical short circuit fault among any generally located links. We have succeeded in conclusively diagnosing short circuit fault between two links of a baseline network.

The fault diagnosis of short circuit fault in a group of three links has also been completed, with the aim at solving the general problem. As the conclusions in section 3.7 indicate, the number of subcases for higher order short circuit fault (i.e. more than three short circuited circuited links in a group)increase rapidly and more importantly, it subsumes the fault behaviour of the lower order cases. Hence we could not pursue the problem for higher order.

The results of this study summarised are as follows :

1. Short circuit fault needs at most $2\lceil \log_2 N \rceil$ tests for detection, in an NxN network having only S-mode and X-mode valid states of its SEs.

2. A baseline network with a two-link short circuit fault needs at most $4\lceil \log_2 N \rceil + 4$ tests for diagnosis.
3. A baseline network with a three-link short circuit fault needs at most $4\lceil \log_2 N \rceil + 6$ tests for diagnosis.
4. The short circuit fault can be distinguished from single SE fault except in a few cases.

3.2 Fault Model, Upper Bound on the Number of Tests and Test Vector Generation

The logical value of a short circuited link is denoted by Φ (c.f. def.2). The paths on which the short circuited links lie will give a Φ response at the corressponding outputs when the test vector provides complementary test inputs to these paths and the short circuited links lie on different paths. The short circuit fault becomes transparent otherwise. This can be confirmed by a simple example of a 4x4 baseline network shown in fig. 13.

Thus the short circuit fault behaviour can be characterised as :

a) Fault is visible when the short circuited links lie on different paths which receive complementary inputs.
b) Fault is transparent when either the short circuited links lie on different paths which receive same test inputs or the short circuited links lie on the same path.

Upper bound on the number of tests :

Since we assume that the value of Φ is an arbitrary but consistent assignment of 0 or 1, whenever a short circuit fault is visible with a given test vector, the faulty response will be observed only at some of the paths involved in the short circuit. To get hold of the other faulty paths we use the test strategy of testing the network in the same control setting with the complementary test vector. This is similar to the pair of tests in S-phase and X-phase discussed in definition 4.

Henceforth, we will always bear in mind that *'For a visible short circuit fault at least two faulty outputs will be observed with complementary test vectors.'*

Therefore to test for a short circuit fault we need to ensure that all pairs of links in the network receive complementary test inputs.

Lemma 1 : For an NxN MIN having S-mode and X-mode as valid states of its SEs, at most $\lceil \log_2 N \rceil$ test vectors are needed to ensure that all pairs of links belonging to the *same stage* receive complementary test bits.

Proof : Let f(k) be the number of test vectors needed for the stated purpose. Our goal is to find f(N).

Now any test vector applied to an NxN MIN will have k 0's and (N-k) 1's, $0 \le k \le N$. With such a test vector all such pair of links of the input side one of which receives a 0 test bit and the other a 1, get tested for short circuit fault. Further tests are required to test short circuit fault among the group of links that received a 0 (size k) and the group that received a 1 (size N-k) independently. Hence we can write the following recurrence relation :

$$f(N) \le 1 + \min_{0 \le k \le N} (\max (f(k), f(N-k)))$$

Clearly, as f(k) is a nondecreasing function the optimum value of k is $\lceil N/2 \rceil$, so that

$$f(N) \le 1 + f(\lceil N/2 \rceil)$$

The solution of this equation is $f(N) \le \lceil \log_2 N \rceil$.

Thus it can be concluded that all the pairs of input lines of a MIN can be provided complementary test bits using at most $\lceil \log_2 N \rceil$ test vectors.

Now in any MIN having S-mode and X-mode as valid states of its SEs, all links of any stage have a one-one corressponding with the links of the input side. Hence any pair of links belonging to the same stage will receive complementary test bits when their corressponding links at the input side do so. This concludes the proof.

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This upper bound cannot be improved because at least $\lceil \log_2 N \rceil$ test vectors are necessary to guarantee complementary test bits to any pair of links of the *same stage*.

Lemma 2 : For the baseline network :

i) any two paths, one in S-phase and the other in X-phase share at most one link in common and and

ii) if two links lie on the same path in one of the phases, they lie on different paths in the other phase.

Proof : Let the network have N input/output lines, $N=2^n$.

1. Let P be a path in S-phase and Q be a path in X-phase. Let $P_o=(p_{n-1}\ldots p_o)_o$ and $Q_o=(q_{n-1}\ldots q_o)_o$ be their stage 0 links respectively. The proof is by contradiction.

Assumption : Let P,Q share more than one link, say one at stage i and the other at stage j, $0\le i,j\le n$, where stage n denotes the output side. Then addresses of the links P_i, Q_i and P_j, Q_j lying on the path P,Q respectively will be

$P_i=p_o\ldots p_{i-1}p_{n-1}\ldots p_i$ and $Q_i=\bar{q}_o\ldots\bar{q}_{i-1}q_{n-1}\ldots q_i$, . . .(a)

$P_j=p_o\ldots p_{j-1}p_{n-1}\ldots p_j$ and $Q_j=\bar{i}_o\ldots\bar{q}_{j-1}q_{n-1}\ldots q_j$. . . .(b)

w. l. o. g., let i<j and since $P_i=Q_i$ and $P_j=Q_j$ equating the corresponding bits we get

$p_m=q_m$, $i\le m\le j-1$, (from (a))

$p_m=\bar{q}_m$, $i\le m\le j-1$, (from (b))

contradiction!

Therfore P,Q share at most one link.

If they do share one link, say at stage i, $0\le i\le n$, then the addresses of input links of P,Q are related as :

$p_m=q_m$, $i\le m\le n-1$,

$p_m=\bar{q}_m$, $0\le m\le i-1$. . . .(3.2.1)

2. This proof follows directly from 1. For if the two links did not lie on different paths in the other phase then one path in S-phase and the other in X-phase will share two links contradicting 1.

Q. E. D.

Definition 7 : Call two paths *intersecting*, if they share a common link.

Obviously the intersecting paths must be from different control settings of the MIN. Fig.14 shows intersecting paths in baseline and Benes network. In fig.14(a) P is the path in

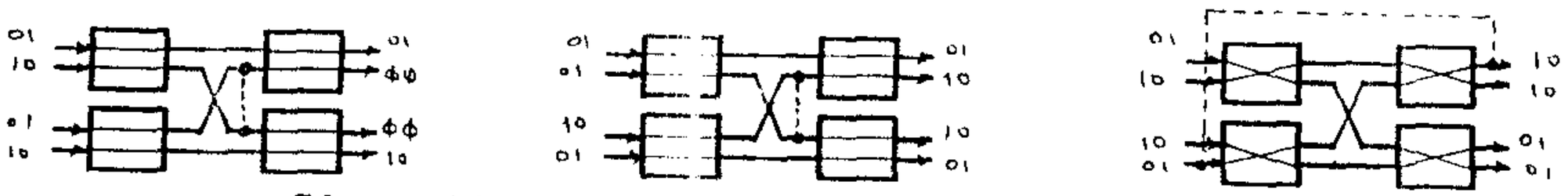


Fig. 13. Short circuit fault model.
(a)Visible fault. (b)Transparent fault.

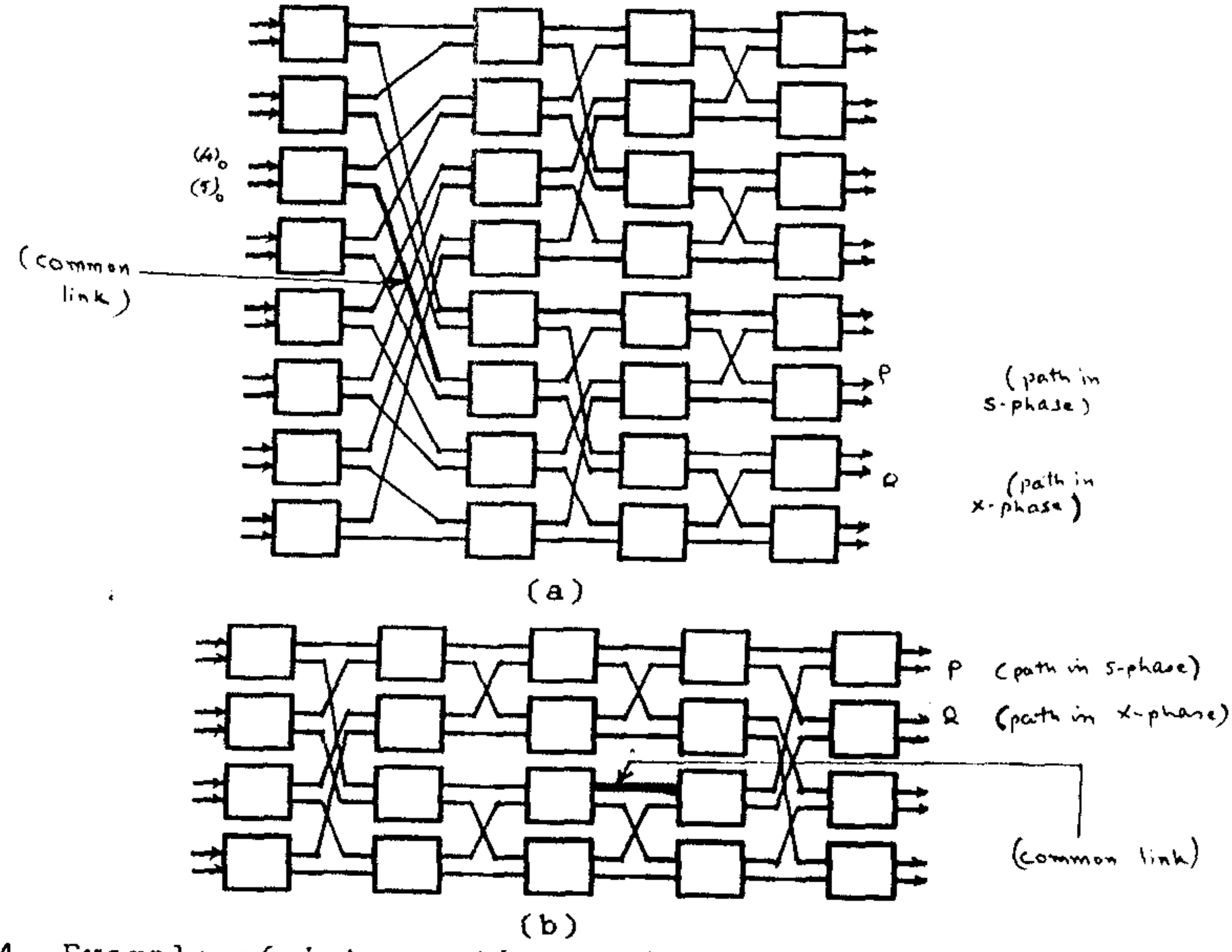


Fig.14. Example of intersecting paths in baseline and Benes networks.

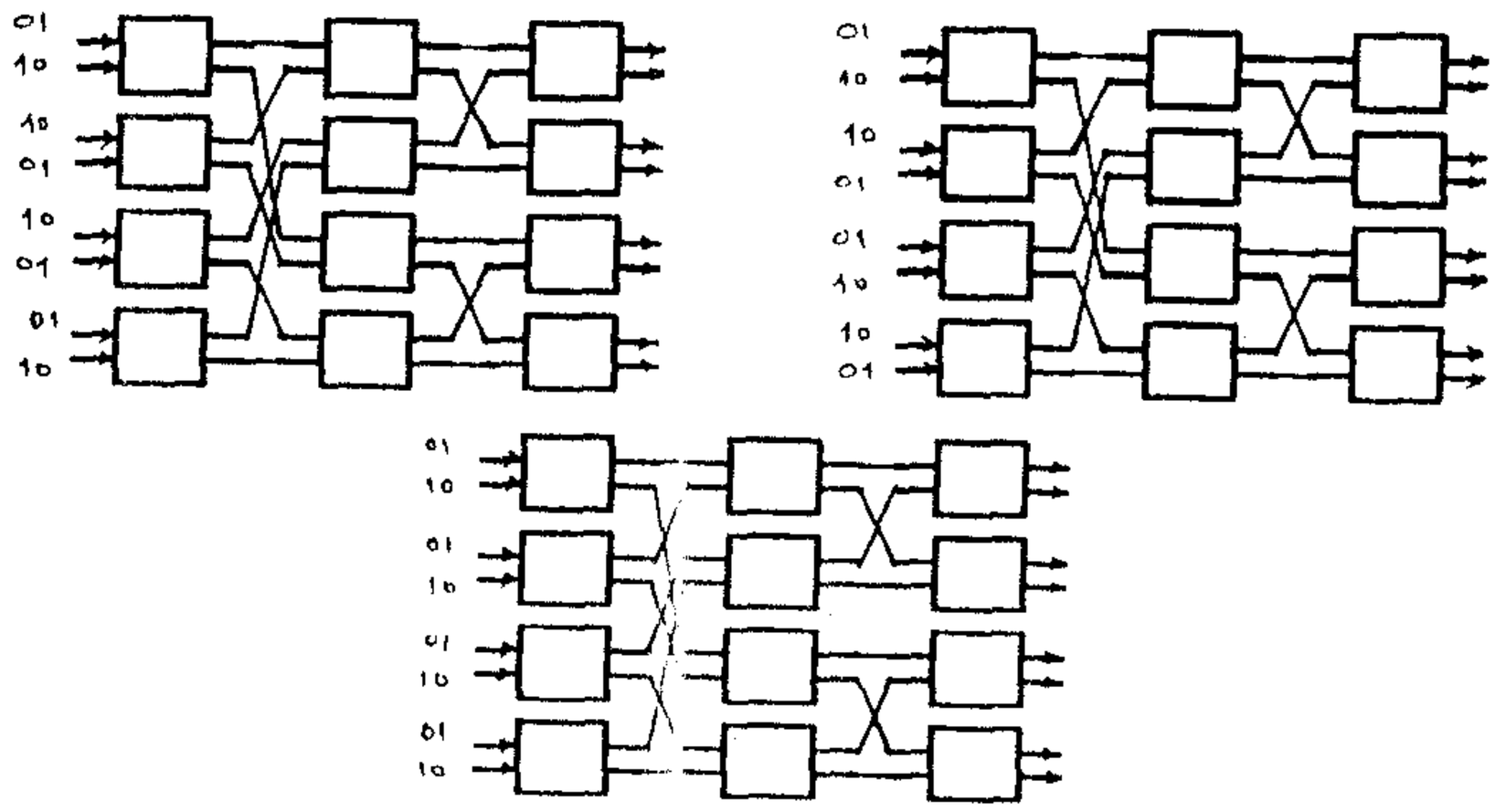


Fig 15. Test vectors generated by algorithm A.

S-phase with input side address $(5)_o$, and Q is th path in X-phase with input side address $(4)_o$.

Theorem 3 : Short circuit fault in baseline and Benes network can be detected in at most $2\lceil \log_2 N \rceil$ tests.

Proof : Lemma 1 gives the upperbound on the number of test vectors that will ensure complementary test bits to any pair of links that belong to the same stage.

Now for any MIN having S-mode and X-mode as valid states of its SEs, there is a one-one correspondence ,in any control setting of the MIN, between a link of the MIN and an input line of the MIN given by the mapping :

g : any link L ⟶ input link of the path containing L.

So any two links L and L' will receive complementary test bits when g(L) and g(L') do so. If g(L) = g(L') then the fault becomes transparent.

So any pair of links that lie on different paths in any control setting of such a MIN will receive complementary test bits in at most $\lceil \log_2 N \rceil$ tests.

Choosing the S-phase as the MIN control setting, lemma 2 ensures that any pair of links will lie on different paths in at least one of S-phase and X-phase.

Hence in particular, the short circuit fault in baseline and Benes network can be detected in at most $2\lceil \log_2 N \rceil$ tests.

Q. E. D.

The following algorithm generates the test vectors for detecting single short circuit as well as single SE fault.

Algorithm D : Test vectors to test NxN baseline network, $N=2^n$

```
1.   For i = n downto 1 do
2.              Classify the input lines into odd and even
                lines based on the i-leftmost bits of their
                address.
3.              Even lines receive a test bit 1, odd lines
                receive a test bit 0.
     endfor
end.
```

Fig.15 gives the test vectors generated for a 8x8 baseline.

3.3 Diagnosis of Single Fault of Baseline Network

We now discuss the diagnostic procedures for single short circuit fault jointly with the SE fault. The first iteration of algorithm D generates the same test vector as that of algorithm A. The test procedure is modified as follows :

(i) For every test vector generated by algorithm D, test the network with that test vector and its complement in both S-phase and X-phase.

(ii) Based on the discussion in sec 3.4 and 3.5 additional tests are done appropriately for diagnosing the fault.

end.

Note that if single SE fault exists, it will be observed with the test vector generated in the first iteration of algorithm D itself. During any subsequent tests, if we observe a faulty output, only then its complementary test is required to get hold of all the faulty paths. Otherwise, the complementary test of the subsequent tests can be skipped.

The test procedure discussed above will cause at least two faulty output responses in a phase if the fault is visible in that phase with the given test vector. A single short circuit fault can have k-short circuited links, $2 \leq k \leq N\log_2 N$. We have studied and given fault diagnosis procedures for k=2 and k=3. The conclusions of section 3.7 discuss the difficulties for k > 3.

3.4 Short Circuit Fault among Two Links in Baseline Network

The fault can be classified on the basis of output responses as follows :

1. Nonseperated two-response fault : There are two faulty outputs in one phase, the other phase is fault-free.
2. Four-response fault : There are two faulty outputs in each phase.

3.4.1 Diagnosis of Nonseperated Two-response Fault

This type of faulty response is also provided by the single SE fault in the union of the sets $\{S_0, S_1, S_4, S_5, S_6, S_7, S_9, S_{13}, S_{15}\}x\{S_5\}$ and $\{S_{10}\}x\{S_0, S_2, S_8, S_9, S_{10}, S_{11}, S_{14}, S_{15}\}$.

In a two-link short circuit case this behaviour implies that the two short circuited links lie on the same path in the fault-free response phase.

The diagnosis is based on the following facts :

(i) If at least one of the faulty response is binary, the fault is of the single SE type, namely one of $(S_1, S_4, S_5, S_7, S_{13})x(S_5)$ or $(S_{10})x(S_2, S_8, S_{10}, S_{11}, S_{14})$.

(ii) If the faulty paths do not converge to a single SE then the fault is of short circuit type.

(iii) If the faulty paths converge to an SE, test the SE by algorithm C for open and short condition of faulty paths. If at least one of the paths is open circuit, the faulty is of the single SE type,namely one of $(S_0, S_6, S_9)x(S_5)$ or $(S_{10})x(S_0, S_6, S_9)$

(iv) If the above cases are inconclusive then the single SE and two-link short circuit fault are indistinguishable as shown in fig.16, since the responses are identical to all tests.

Link identification

If from the above cases we are able to resolve between short circuit fault and SE fault then the short circuited links must be identified.

Theorem 4 : Given two paths P,Q of a baseline network in one phase, there are exactly two paths in the other phase which intersect both P and Q.

Proof : Let $P_0=p_{n-1}\ldots p_0$ and $Q_0=q_{n-1}\ldots q_0$ be the stage-0 links of paths P,Q respectively in an NxN baseline network, $N=2^n$. w. l. o. g. let P,Q be paths in the X-phase.

We want to find all such paths, A, in S-phase that intersect both P and Q. Let $A_0=a_{n-1}\ldots a_0$ be the stage-0 link of A and let it intersect P,Q at stage-i and stage-j respectively, $0\le i,j\le n$.

Then by equation (3.2.1) we have

$a_m=\overline{p}_m$, $0\le m\le i-1$, and $a_m=p_m$, $i\le m\le n-1$,

$a_m=\overline{q}_m$, $0\le m\le j-1$, and $a_m=q_m$, $j\le m\le n-1$,

Therefore $p_m=\bar{q}_m$, $0\le m\le \min(i,j)-1$ and $\max(i,j)\le m\le n-1$

$p_m=q_m$, $\min(i,j)\le m\le \max(i,j)-1$

Thus P and Q must have a definite bit pattern and they are mutually dependent.

Now either i<j or j<i

Accordingly $A_o=p_{n-1}\ldots p_j p_{j-1}\ldots p_i \bar{p}_{i-1}\ldots \bar{p}_o$ for i<j

in which case $Q_o=p_{n-1}\ldots p_j \bar{p}_{j-1}\ldots \bar{p}_i p_{i-1}\ldots p_o$

or $A_o=p_{n-1}\ldots p_i \bar{p}_{i-1}\ldots \bar{p}_j \bar{p}_{j-1}\ldots \bar{p}_o$ for j<i

in which case $Q_o=p_{n-1}\ldots p_i \bar{p}_{i-1}\ldots \bar{p}_j p_{j-1}\ldots p_o$

Hence the theorem is proved. The four paths have the following address pattern

S-phase	X-phase
$p_{n-1}\ldots p_j p_{j-1}\ldots p_i \bar{p}_{i-1}\ldots \bar{p}_o$,	$p_{n-1}\ldots p_j p_{j-1}\ldots p_i p_{i-1}\ldots p_o$
$p_{n-1}\ldots p_j \bar{p}_{j-1}\ldots \bar{p}_i \bar{p}_{i-1}\ldots \bar{p}_o$,	$p_{n-1}\ldots p_j \bar{p}_{j-1}\ldots \bar{p}_i p_{i-1}\ldots p_o$

Q.E.D.

From theorem 4, we can conclude that *'In a nonoperated two response behaviour of a two-link short circuit fault, the pair of shorted links may lie on one of exactly two paths in the fault free phase.'* . . .(3.4.2)

Fig.17(a) shows an example of this fault. The S-phase is fault-free and X-phase is faulty. The fault is observed with the third test vector, in which, paths $(0)_0$ and $(6)_0$ show faulty response. So either the links $(8)_1$ and $(8)_9$ are short circuited or the links $(11)_1$ and $(14)_9$ are short circuited.

From equation (3.4.2) it can be seen that there are two possible locations of the fault namely, one link of the i^{th} stage and one link of the j^{th} stage, as shown in fig.18. Either (A_i,A_j) or (B_i,B_j) is the short circuited pair of links. We set the stages 0 to i in the fault-free response phase and the remaining stages in the other phase. This ensures that all the links A_i,A_j,B_i and B_j lie on different paths. Test the paths containing (A_i,A_j) for short circuit behaviour. If the response is fault-free (B_i,B_j) is the faulty pair of links, else (A_i,A_j) is the faulty pair of

Fig. 16. Non seperated two-response fault : undistinguishable SE and two-link short circuit fault. (a)Fault observed in S-phase. (b)Fault observed in X-phase.

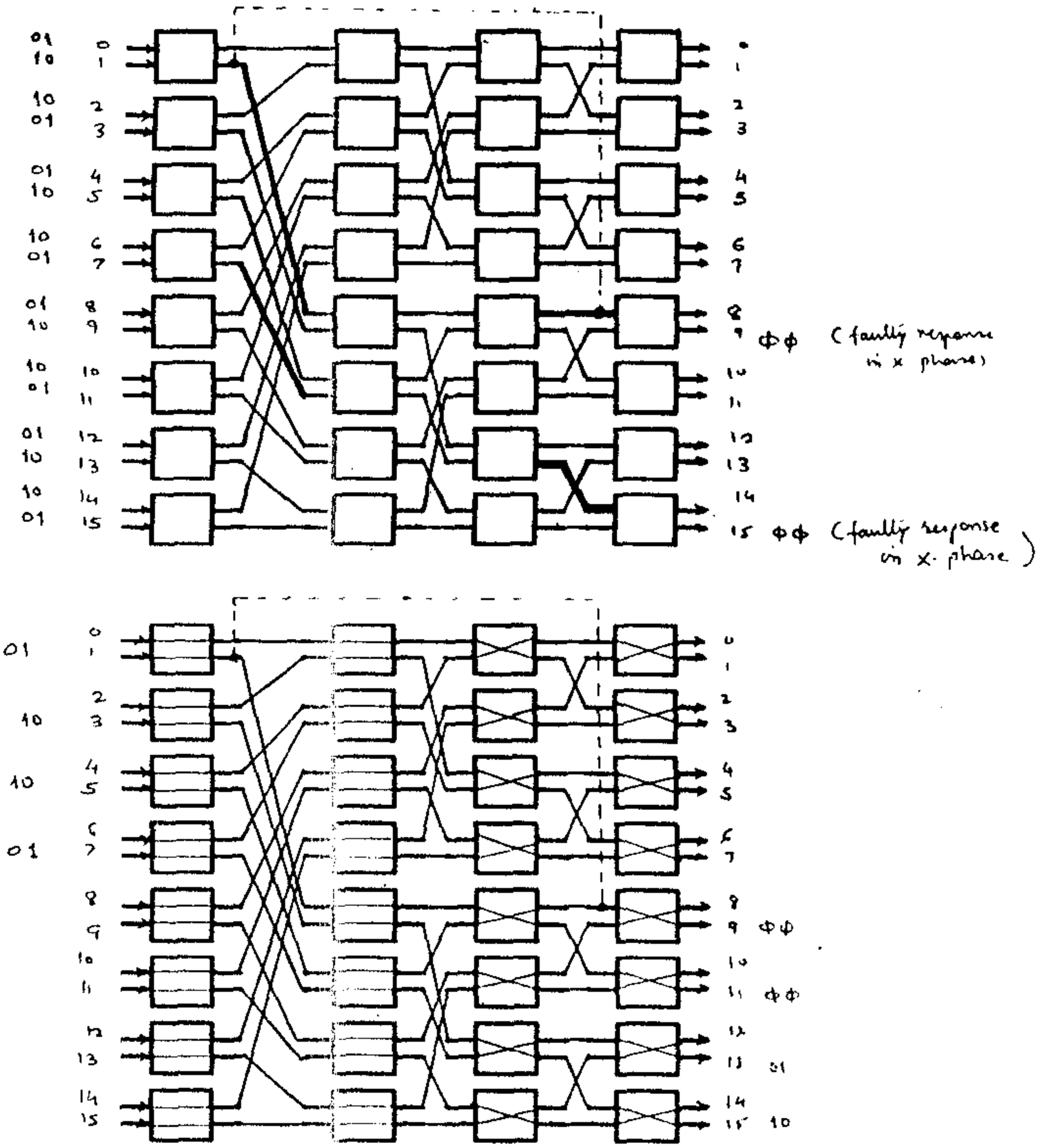


Fig. 17. Nonseperated two-response short circuit fault. (a)Fault detection. Possible fault location is $(8)_1,(8)_3$ or $(11)_1,(14)_3$. (b)Fault identification tests.

links. The fault location requires 2 tests.

This fault therefore requires at most $4\lceil \log_2 N \rceil + 4$ tests for diagnosis. Fig17(b) shows the link identification tests for the fault example of fig.17(a).

3.4.2 Diagnosis of Four-response Fault

This type of faulty response is also provided by the single SE fault in the set$(S_0, S_1, S_4, S_5, S_6, S_7, S_9, S_{13}, S_{15}) \times (S_0, S_2, S_6, S_8, S_9, S_{10}, S_{11}, S_{14}, S_{15})$. In a two-link short circuit case this behaviour implies that the two short circuited links lie on different paths in both phases.

The diagnosis is based on the following facts :

(i) If at least one of the faulty response is binary, the fault is of the SE namely one of $(S_1, S_4, S_5, S_7, S_{13}) \times (S_2, S_8, S_{10}, S_{11}, S_{14})$.

(ii) If the faulty paths of the same phase do not converge to a single SE then the fault is of short circuit type.

(iii) If the faulty paths of the same phase converge to an SE (the other pair of faulty paths will also converge to the same SE), test the SE by algorithm C for open and short condition of faulty paths. If at least one of the paths is open circuit, the faulty is of the SE namely one of $(S_0, S_6, S_9) \times (S_0, S_6, S_9)$

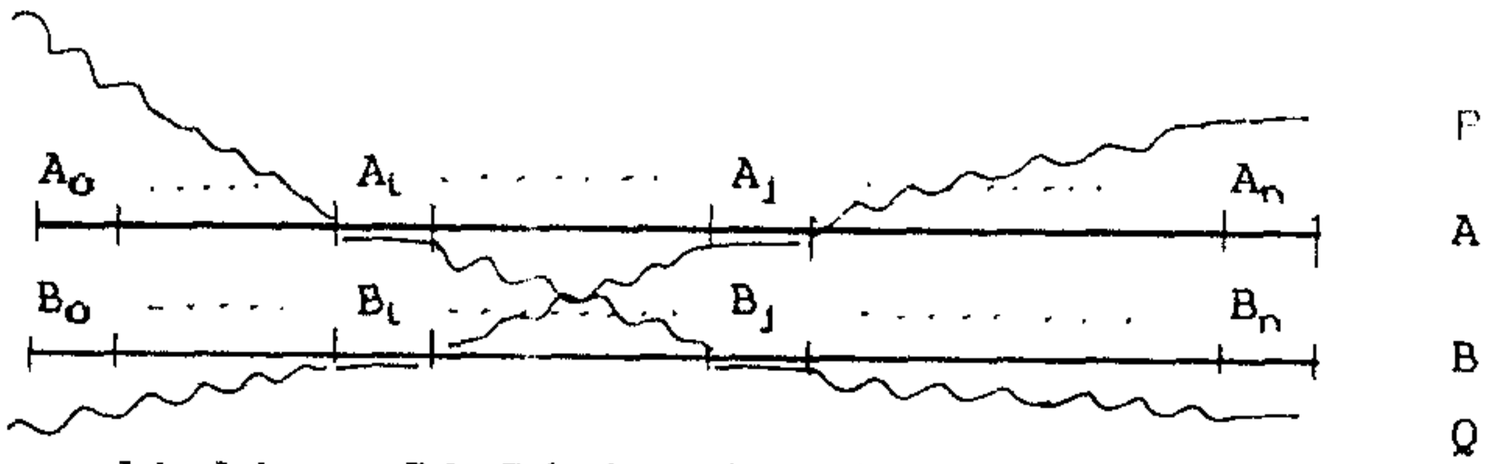
(iv) If the above cases are inconclusive then the fault is indistinguishable at the SE and two-link short circuit level as shown in fig.19, since the responses are identical to all tests.

Link identification

Let P,Q be the X-phase faulty output paths and A,B be those in the S-phase. Then based on the addresses of P,Q,A and B the following subcases arise :

1. Each of A,B intersects exactly one of P,Q respectively. Let a intersect P and B intersect Q. Here neither P,Q nor A,B satisfy equation (3.2.1).

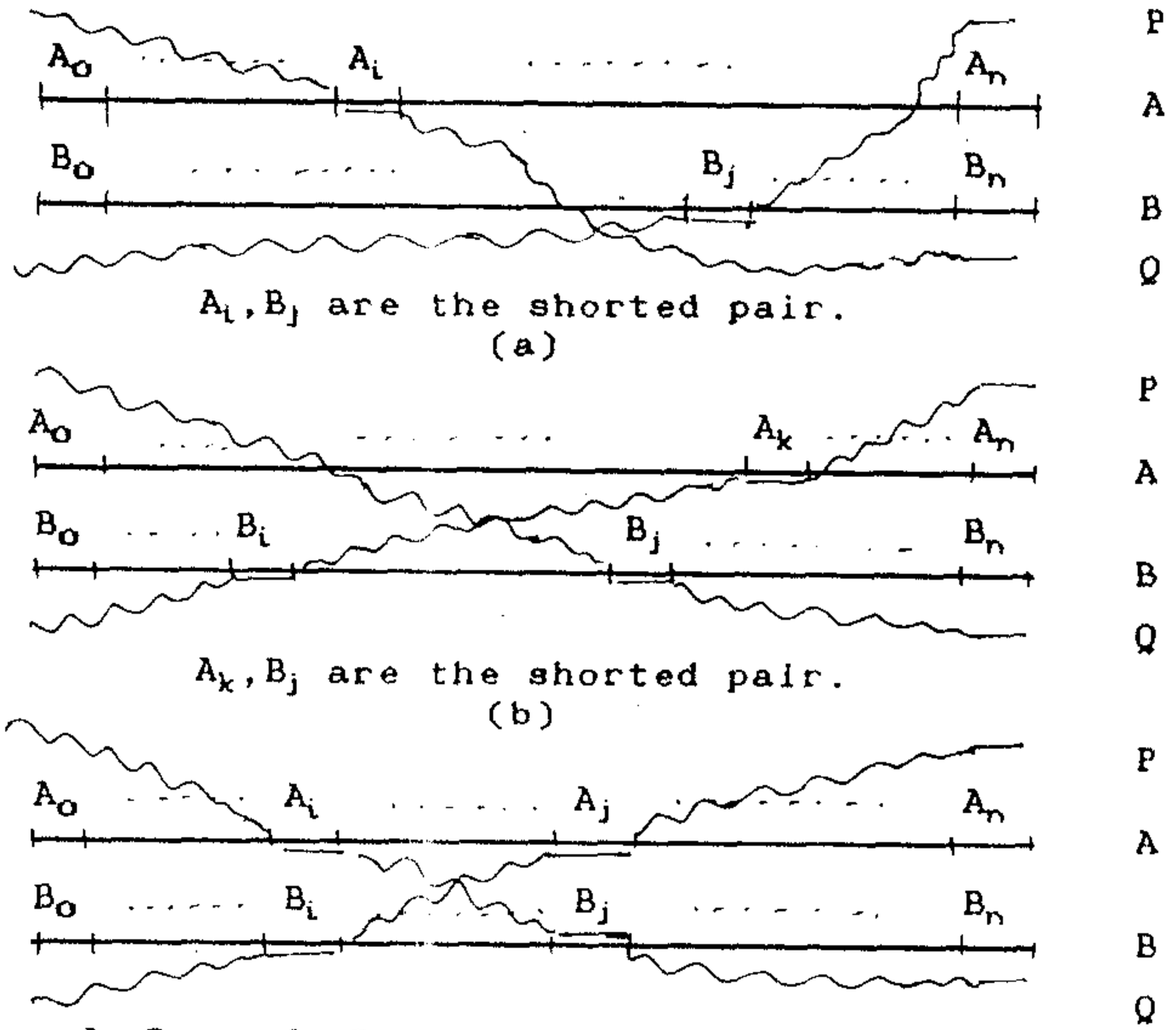
2. One of A,B intersects both P,Q the other intersects only one of P,Q. Let B intersect P,Q and A intersect P only. Here only P,Q equation (3.2.1).



Ai,Aj or Bi,Bj is the shorted pair
PP,Q : paths which show faulty response.
A,B : paths in the fault free phase.

Fig. 18. Short circuit fault locations in nonseperated two-response fault.

Fig. 19. Four-response fault : undistinguishable SE and two-link short circuit fault.



A_i, B_j are the shorted pair.
(a)

A_k, B_j are the shorted pair.
(b)

A_i, B_i or A_j, B_j are the shorted pairs.
(c)
A,B : faulty paths in S-phase.
P,Q : faulty paths in X-phase.

Fig. 20. Short circuit fault location in four-response fault.

3. Both A,B intersect P and Q. Here both P,Q and A,B satisfy equation (3.2.1).

Case 1 : This situation is shown in fig.20(a). The pair of short circuited links are directly identified by determining the common links of A,P and B,P.

Case 2 : . This situation is shown in fig.20(b) The short circuited links will be : the common link of (A,P) and the common link of (B,Q).

Case 3 : As discussed in section 3.4.1, the addresses of A,B,P,Q at the input side will confirm with equation (3.4.1). From fig.20(c) it can be seen that either (A_i, B_i) or (A_j, B_j) is the short circuited pair of links. Once again by setting the stages 0 to i in S-mode and the rest in X-mode, A_i, B_i, A_j and B_j will be in different paths and the short circuited pair of links can be located in two tests.

This fault therefore also requires at most $4\lceil \log_2 N \rceil + 4$ tests for diagnosis.

3.6 Short Circuit Fault among Three Links in Baseline Network

The fault can be classified on the basis of output responses as follows :

1. Nonseperated three-response fault : There are three faulty outputs, all in one phase. The other phase is fault-free.
2. Five-response fault : There are three faulty outputs in one phase and two faulty responses in the other phase.
3. Four-response fault : There are two faulty responses in each phase.
4. Six-response fault : There are three faulty outputs in each phase of testing.

As mentioned in section 3.2, there is no occurrence of single faulty output in short circuit fault. Each of these cases are discussed in the following paragraphs.

3.5.1 Diagnosis of Nonseperated Three-response Fault

This fault behaviour is absent in the two-link short circuit and single SE fault case. In this case the three short circuited links lie on the same path in the fault-free

case and on different paths in the faulty phase.

Link identification

Theorem 5 : Given three links in a baseline network which, lie on different paths in one phase, there exists exactly one path in the other phase on which all three links will lie.

Proof : Consider an NxN baseline network, $N=2^n$. Let P,Q and R be the three paths with input links $P_o=(p_{n-1}...p_o)_o$, $Q_o=(q_{n-1}...q_o)_o$ and $R_o=(r_{n-1}...r_o)_o$ respectively. w. l. o. g., let P,Q,R be links in K-phase.

We want to find all such paths, A, in S-phase that intersect P Q and R. Let $A_o=a_{n-1}...a_o$ be the stage-0 link of A and let it intersect P,Q,R at stage-i stage-j and stage-k respectively, $0\leq i,j,k\leq n$.

Then by equation (3.2.1) we have

$a_m=\overline{p}_m$, $0\leq m\leq i-1$, and $a_m=p_m$, $i\leq m\leq n-1$,

$a_m=\overline{q}_m$, $0\leq m\leq j-1$, and $a_m=q_m$, $j\leq m\leq n-1$,

$a_m=\overline{r}_m$, $0\leq m\leq k-1$, and $a_m=r_m$, $k\leq m\leq n-1$,

w. l. o. g., $i<j<k$ be the ordering of i,j and k.

Then equating the corressponding bits in the above equation we have :

$\overline{p}_m=\overline{q}_m=\overline{r}_m$, $0\leq m\leq i-1$ and $k\leq m\leq n-1$

$p_m=\overline{q}_m=\overline{r}_m$, $i\leq m\leq j-1$, . . . (3.5.1)

$p_m=q_m=\overline{r}_m$, $j\leq m\leq k-1$,

From equation (3.5.1) we see that P,Q,R must have a definite bit pattern in which the whole address can be divided into four consecutive blocks. The bits in the first and the last block starting from the lsb are exactly same, while in the second and the third ones the bit pattern of two paths are exactly same while that of the other is their complement. Note that the address of A gets fixed once the intersection stage with any of the lines gets determined. Also $i\geq 0$ and $k\leq n$, but i,j,k are all distinct. Hence knowing the input side address of the faulty paths, the stage at which a link is first shared can be determined by scanning

the addresses from the lsb and picking the path whose bits are complementary compared to the other two. Thus there is exactly one address for path A.

Q.E.D.

For the case of P,Q,R being paths in the S-phase the theorem can be similarly proved. They will again satisfy equation (3.5.1) and the address of path A can be easily determined.

Link identification

The short circuited links can be identified by the method proposed in theorem 5. Scan the addresses of the faulty paths from the lsb. These addresses will confirm with the bit pattern of equation (3.5.1). From these the values of i,jand k will be uniquely obtained and thus the short circuited links are identified. Fig.21 gives an example of this fault.

3.5.2 Diagnosis of Five-response Fault

This fault behaviour is absent in the two-link short circuit and single SE fault case. In this case the three short circuited links all lie on different paths in one phase and in the other phase two of the links lie on the same path.

Link identification

If two links of paths P,Q of one phase lie on the same path in other phase, then by equation (3.2.1) the input side addresses of P,Q will have the form

$$p_m = q_m \quad , 0 \le m \le i-1 \text{ and } j \le m \le n-1$$

$$p_m = \bar{q}_m \quad , i \le m \le j-1. \qquad \ldots (3.5.2)$$

In this case let the three-response phase paths be denoted by A,B,C and those of the two-response phase paths be denoted by P,Q.

Now if exactly two of A,B,C, say A,B, satisfy the address bit pattern of equation (3.5.2) then only one of P,Q, say P, will intersect both A,B and Q will intersect only C. The links are thus identified.

If more than one pair of links among A,B,C satisfy the

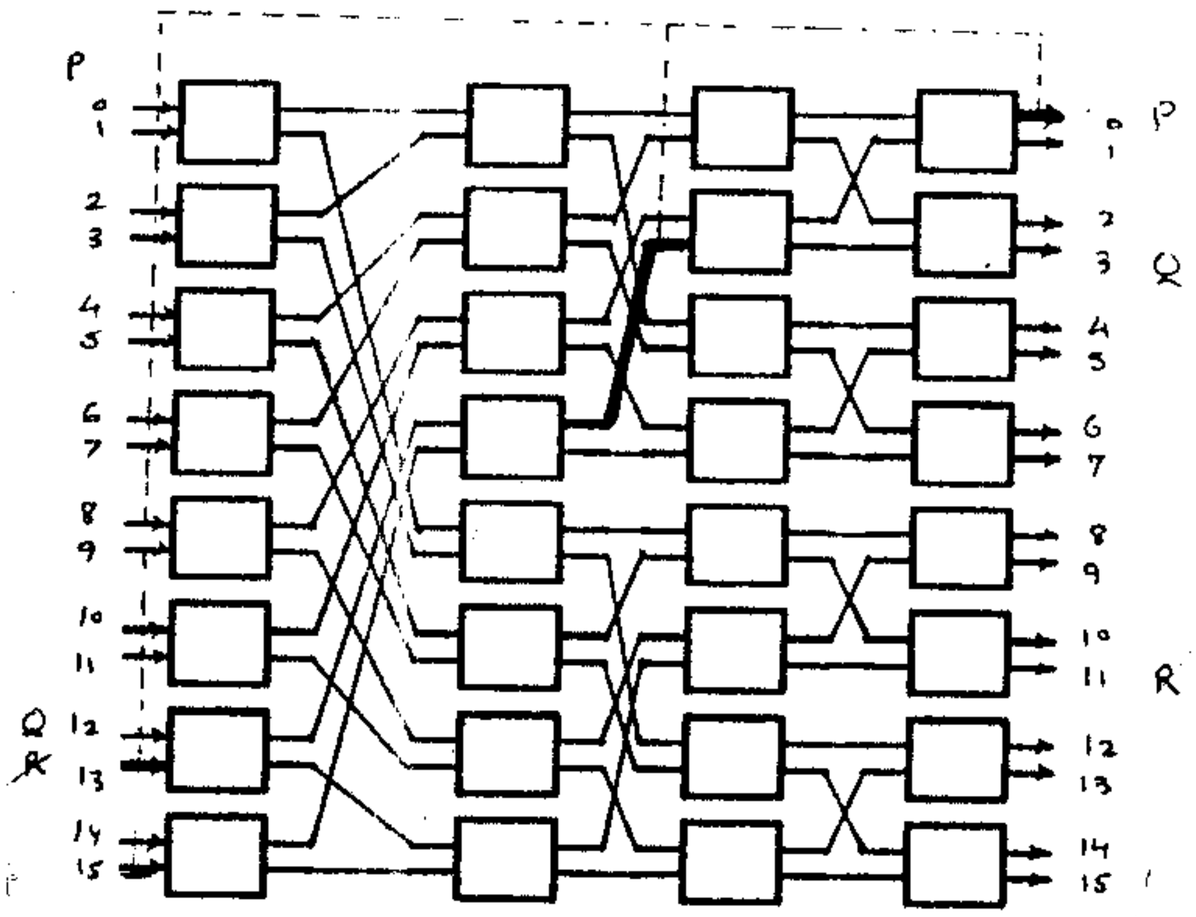


Fig.21 Non-seperated three-response fault.

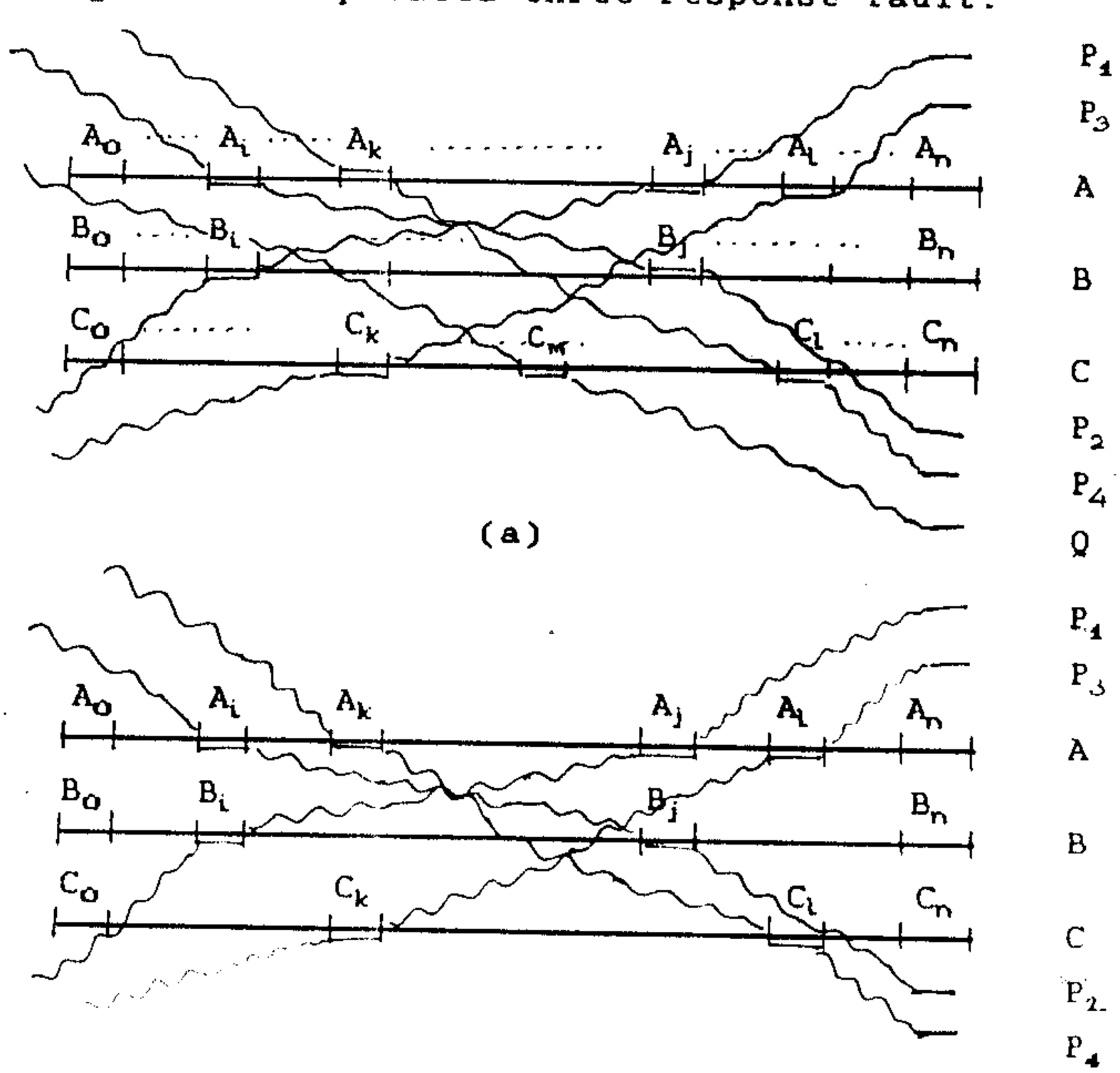


Fig.22. Link identification of five-response fault.

bit pattern of equation (3.5.2), then it is easy to see that all the three possible pair of links cannot satisfy equation (3.5.2) for, in that case it would degenerate to the type 3.5.1. So we are left with the situation that two pair of links among A,B,C satisfy the bit pattern of equation (3.5.2).

Let the two pair of paths be A,B and A,C. Then there are two lines P_1, P_2 in the other phase which intersect A and B and two lines P_3, P_4 which intersect A and C. Now either both or exactly one of $P,Q \in S=(P_1, P_2, P_3, P_4)$.

If exactly one of P,Q ,say P, belongs to S then P intersects one pair of A,B,C and Q intersects with the remaining path. The links are thus identified as shown in fig. 22(a).

If both P,Q are in S then w. l. o. g. let $P \in (P_1, P_2)$ and $Q \in (P_3, P_4)$, noting that P and Q cannot be in the same partition of S. Let $P=P_1$ and $Q=P_3$. Then the faulty links are either A_j, B_i, C_k or A_i, B_i, C_k shown in fig.22(b). This can be resolved by one additional test in which the SEs in the stage 0 to 1 are set in S-phase and the rest are set in X-phase. *The fault is indistinguishable if* $|i-j|=1$. This case can therefore be diagnosed in two additional tests.

3.5.3 Diagnosis of Four-response Fault

This fault behaviour is also observed in the two-link short circuit and single SI fault case. In this case, in both phases two short circulted links will lie on one path and the other on the remaining path.

Link identification

Let A,B be faulty output response paths in S-phase and P,Q be those in X-phase. If both P,Q and A,B do not satisfy equation (3.5.2). then the fault certainly does not invlove three short circuited links and belongs to 3.4.2 subcase 1. This is because in the three short circuit link case, such a behaviour implies that two short circuited links lie on one path in each phase.

If only one pair of links among P,Q and A,B satisfy equation (3.5.2), then the fault is of the type 3.4.2 subcase 2, as shown in fig.18(b). If two-links are short circuited , (A_k,B_j) are the faulty links. If three links are short circuited, A_k,B_i,B_j are the faulty links. Thus to resolve between these two faults, we have to determine if B_i is involved. This can be determined by seperating the links into different paths i.e. setting stages 0 to i in S-phase and the rest in X-phase. *If* k=i+1 or j=i+1 *then the two-link and three short circuit fault are indistinguishable.*

If both P,Q and A,B satisfy equation (3.5.2) (i.e. k=i or j in fig.18(b)) then from fig.18(c) it can been seen that in the three-link short circuit case any three of A_i,A_j,B_i and B_j may be faulty (# four groups). In other words we have to determine which three of the four links are mutually short circuited. By lemma 1 this can be done in two additional tests by forcing these links into different paths. Again *if* j=i+1 *the fault is indistinguishable.*

Thus this fault requires at most four tests for diagnosis.

3.5.3 Diagnosis of Six-response Fault

This fault behaviour is absent in the two-link short circuit and single SE fault. In this case all the short circuited links lie on different paths in both phases.

Link identification

This fault can be subdivided into many subcases depending on the addresses of the faulty paths. But basically it can be diagnosed as follows : Any faulty path of a phase will intersect with at least one faulty path of the other phase. Find all the common links. Then among these links the short circuited group can be identified by forcing these links in different paths

This completes the discussion of the three link short circuit fault considered jointly with the two-link short circuit fault and SE fault. It has been shown that most faults are diagnosable. The faults in which the input-output

links of an SE are involved are indistinguishable. The diagnosis requires at most six tests after detection.

3.6 Short Circuit Fault Diagnosis of Benes Network

Here we want to highlight the fact that the short circuit fault diagnosis techniques discussed for baseline network can be applied almost unmodified to fault diagnosis of the Benes network too. The single SE fault diagnosis problem of Benes network has not been dealt with so far in the literature because of the presence of alternate paths between any input-output pair ([A82] and [FY86]). However it is significant that the short circuit fault can be diagnosed for the Benes ntework without much modification.

Lemma 3 : For the Benes network :

i) two paths, one in S-phase and the other in X-phase share at most one link in common, and

ii) if two links lie on the same path in one of the phases,they lie on different paths in the other phase.

Proof : Let the network have N input/output lines, $N=2^n$.

1. The Benes network is symmetric about the stage n, and can be visualised as two NxN baseline networks connected back to back.

By (I) paths P,Q cannot share more than one link in any of the two halves comprising of stages 0 to n-1 and stages nto 2n-1, where stage 2n-1 is the output side. Hence it is enough to show that if paths P,Q share a link in the first half they cannot do so in the second half, the symmetry takes care of the inverse proposition.

By equation (3.2.1) we have

$p_m = q_m$, $i \leq m \leq n-1$,

$p_m = \bar{q}_m$, $0 \leq m \leq i-1$, where $0 \leq i \leq n-1$, i being the stage where the common link is located.

In Benes network address of the paths at the output side will be $P_{2n} = p_{n-1} p_{n-2} \ldots p_0$ and $Q_{2n} = \bar{q}_{n-1} q_{n-2} \ldots q_0$ respectively.

Thus we have

$P_{2n}=p_{n-1}p_{n-2}\cdots p_i p_{i-1}\cdots p_o$ and $Q_{2n}=\overline{p}_{n-1}p_{n-2}\cdots p_i\overline{p}_{i-1}\cdots\overline{p}_o$

Now looking at the baseline network formed by the second half of the Benes network, P_{2n}, Q_{2n} can be viewed as input lines of this network. We find that for no value of i can the equation (3.2.1) be satisfied. Hence the paths having input lines P_{2n}, Q_{2n} do not share any link in the second half of the Benes network.

2. This proof follows directly from 1. For if the two links did not lie on different paths in the other phase then one path in S-phase and the other in X-phase will share two links contradicting 1.

Q. E. D.

Thus if two paths P,Q in a Benes network share a common link at stage i, their input side addresses will be as follows

$p_m=q_m$, $i\leq m\leq n-1$, $p_m=\overline{q}_m$, $0\leq m\leq i-1$, in which case $0\leq i\leq n-1$ or

$p_m=q_m$, $i\leq m\leq n-2$, $p_m=\overline{q}_m$, $0\leq m\leq i-1$ and $m=n-1$, in which case $n\leq i\leq 2n-1$. . . .3.6.1

If we test the Benes network in the S-phase and X-phase with exactly the same test vectors as those for the baseline network, we shall observe similar faulty response behaviour as those of the baseline network because of lemma 3. From equation (3.6.1) the relations for the intersecting paths are known and the common link can determined from the addresses of the intersecting paths. Based on lemma 3 it is easy to see that theorem 4 and theorem 5 hold for the Benes network too. Therefore the two-link and three short circuit fault can be diagnosed for the Benes network. The only modification is in identifying the faulty links since the common links will be identified by equation (3.6.1) instead of (3.2.1). To avoid repeatition we do not discuss this topic further, but it is emphasised that short circuit fault diagnosis of Benes network is also possible based on our study of short circuit fault diagnosis of baseline network.

3.7 Conclusions

Fault diagnostic procedures for two-link short circuit and three-link short circuit fault considered jointly with single SE fault have been developed. Similar techniques for Benes network have been proposed. The upper bound on the number of test vectors needed for detecting short circuit fault in an NxN network is $\lceil \log_2 N \rceil$. This upper bound cannot be improved because at least $\lceil \log_2 N \rceil$ tests are needed to ensure complementary test bits for any pair of links of the *same stage* in the network.

The fault diagnostic procedures for short circuit fault indicate that some faults are indistinguishable by tests involving access only the input-output terminals of the MIN. These faults involve links that form the input-output links of an SE. The fault detection phase generally provides enough data to locate and identify the fault. Further tests are done if this data is insufficient as discussed in some cases.

The three-link short circuit fault also includes the fault behaviour of the two-link short circuit fault. Moreover the number of subcases increase rapidly as the number of links involved increases. So if we think of dealing with short circuit of higher order, the results for the lower order become incomplete because the new type of fault includes some subcases which behave exactly like those of the lower order type. From the two-link and three link study it does not appear that there is a neat and compact solution for the general k-link short circuit case. In our opinion, the conclusive results for the two-link short circuit case are in themself quiet significant because it can be safely assumed that short circuit faults having more than two links is rare. Assuming that at most two links may be short circuited, the fault diagnosis procedures *complete* the diagnosis of baseline network from a practical viewpoint.

Further study may be undertaken to consider multiple short circuit faults, each fault involving two links. Using the fault diagnosis procedures developed by Feng in [FY86],

the short circuit fault diagnosis of omega^{r}-omega^{-t} network can be pursued. On similar lines, the complete set of fault diagnostic procedures may be developed for shuffle-exchange networks.

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