

Hierarchical Partitioning of VLSI Floorplans by Staircases

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This article addresses the problem of recursively bipartitioning a given floorplan F using monotone staircases. At each level of the hierarchy, a monotone staircase from one corner of F to its opposite corner is identified, such that (i) the two parts of the bipartition are nearly equal in area (or in the number of blocks), and (ii) the number of nets crossing the staircase is minimal. The problem of area-balanced bipartitioning is shown to be NP-hard, and a maxflow-based heuristic is proposed. Such a hierarchy may be useful to repeater placement in deep-submicron physical design, and also to global routing.

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1. INTRODUCTION

Consider a VLSI layout having rectangular boundary, as shown in Figure 1. It consists of a set of rectangular circuit blocks $B = \{b_1, b_2, \dots, b_n\}$, and a set of nets $N = \{\eta_1, \eta_2, \dots, \eta_k\}$, where each block b_i is associated with a list of nets $B_i \subset C$, as shown in parentheses in Figure 1(a). A *net* is a set of electrically equipotential terminals on blocks that are to be interconnected. In the important step of global routing [Burman et al. 1991; Sherwani 1993] for state-of-the-art gigascale technology, a sequence of subregions, or generalized channels, is determined for each net, through which its terminals are to be connected in order to minimize wire length and chip area, as well as congestion. The shape of the regions strongly influences the quality of the solution [Sun et al. 1996].

In a given placement of blocks, a staircase channel may be defined as an empty polygonal region bounded by two monotonically increasing (or decreasing) staircase paths formed by connected isothetic line segments from one corner of the layout to its diagonally opposite corner [Dasgupta et al. 2002]. In Figure 1(a), the region bounded by the pair of dashed line segments is one such staircase channel. A VLSI *floorplan* is often envisaged as a rectangular dissection of a bounding rectangle by isothetic cut lines. For simplicity, we model a *staircase in a floorplan* F by a monotone rectilinear path without any width, as shown in Figure 1(b), from the bottom-left corner of F to its top-right corner. This partitions the set of blocks in F into two parts, namely, *left-set* and *right-set*, respectively. A *mincost staircase cut (MSC)* is a staircase such that the number of distinct nets attached to the blocks on both the *left-set* and *right-set*, is minimum [Majumder et al. 2004]. Monotone staircases, henceforth referred as *ms-cuts* of a floorplan F , have been shown to be particularly advantageous to efficient routing [Guruswamy and Wong 1988; Sur-Kolay and Bhattacharya 1991; Majumder et al. 2004].

A maxflow-based algorithm [Majumder et al. 2004] can determine in polynomial time a series of *ms-cuts* with minimum number of *crossing nets*, that is, distinct nets with terminals on either side. These *ms-cuts* recursively bipartition a given rectangular floorplan until degenerate staircases, that is, straight cutlines are obtained. Thus a hierarchy (binary tree) of *ms-cuts* is defined as shown in Figure 2. In this scheme, the problem of assigning nets to *ms-cuts* is solved by postorder traversal of this binary tree, thereby reducing routing congestion in the longer *ms-cuts* toward the top of the tree. This in turn, saves routing area. More often than not, the above algorithm [Majumder et al. 2004] yields an unbalanced tree, which may reduce the efficacy of the scheme. In general, a balanced physical hierarchy [Chang et al. 2003] is preferable for reducing overall time complexity and congestion. A maxflow-based *balanced* bipartitioning method [King et al. 1995] is employed in this article to obtain a balanced hierarchy of *ms-cuts*, as heuristics like Kernighan-Lin [Sherwani 1993] cannot capture the topological constraints of the floorplan and thus cannot guarantee *ms-cut* geometry.

Two main criteria for balance in floorplan bipartitioning are (a) the number of blocks, and (b) the area of partitions. While the first one affects the depth

2. MOTIVATION FOR THE *MSC* PROBLEM

The *MSC* problem is very pertinent to the repeater placement issues frequently encountered in interconnect-centric floorplanning used for deep-submicron VLSI physical design [Sarkar and Koh 2001; Cong et al. 1999a; Chu and Wong 1997; Okamoto and Cong 1996]. It is also relevant to global routing.

2.1 Repeater Placement Problem

Owing to the continued scaling of VLSI technologies, interconnects appear to play a dominant role in determining system performance, power, reliability, and cost [Cong et al. 1996]. It has been observed that repeater block insertion is one of the most effective methods to optimize signal delay [Cong et al. 1999a; Chu and Wong 1997; Okamoto and Cong 1996]. Judicious insertion of repeaters reduces the delay from quadratic to linear in terms of wire length [Cong et al. 1999b]. Usually, most interconnect synthesis techniques are designed for post-placement interconnect optimization. Over 700,000 repeaters may be needed in a single chip for the 70-nm technology [Cong 1997]. Insertion of many repeaters may significantly change the floorplan and placement of a design, which was optimized earlier in the floorplanning stage. This leads to the problem of designing an efficient routability-driven repeater block placement method. As repeaters for the signal nets are to be placed on the silicon layer, one needs to identify the unoccupied regions on it. A recent method of repeater placement uses monotone paths [Sarkar and Koh 2001] similar to monotone staircase channels. Minimizing the congestion in a monotone staircase channel, and hence the *MSC* problem, has the potential to strongly influence the repeater placement strategy.

In Figure 3 we show how the monotone staircase framework can help in repeater insertion through a typical example. The multiterminal net a in Figure 3(a) has terminals on either side of a monotone staircase region, and it crosses the staircase only once. A repeater has to be inserted within the staircase region whenever the length of the wire crossing the channel exceeds the permissible threshold. Note that the repeater is inserted in the device layer, whereas the wire passing through the repeater is in the metal layer. Further, for any net, there is a feasible region for repeater placement, as indicated in Figure 3(b). It may be necessary to place more than one repeater, either for the same net or for different nets, within the same staircase region depending upon the length of the net(s). If the width(s) of a staircase region is (are) not sufficient (Figure 3(c)) to accommodate all the repeaters required for meeting the timing requirements, the two partitions can be moved apart along the monotone staircase to create more space in the device layer, as shown in Figure 3(d). Monotone staircases offer this advantage as there does not exist any cyclic dependency among the channels in their routing order [Guruswamy and Wong 1988; Sur-Kolay and Bhattacharya 1991]. Hence “rip-up and reroute” is never required during postorder traversal of the staircase tree, even if a particular channel needs to be stretched in order to accommodate more repeaters.

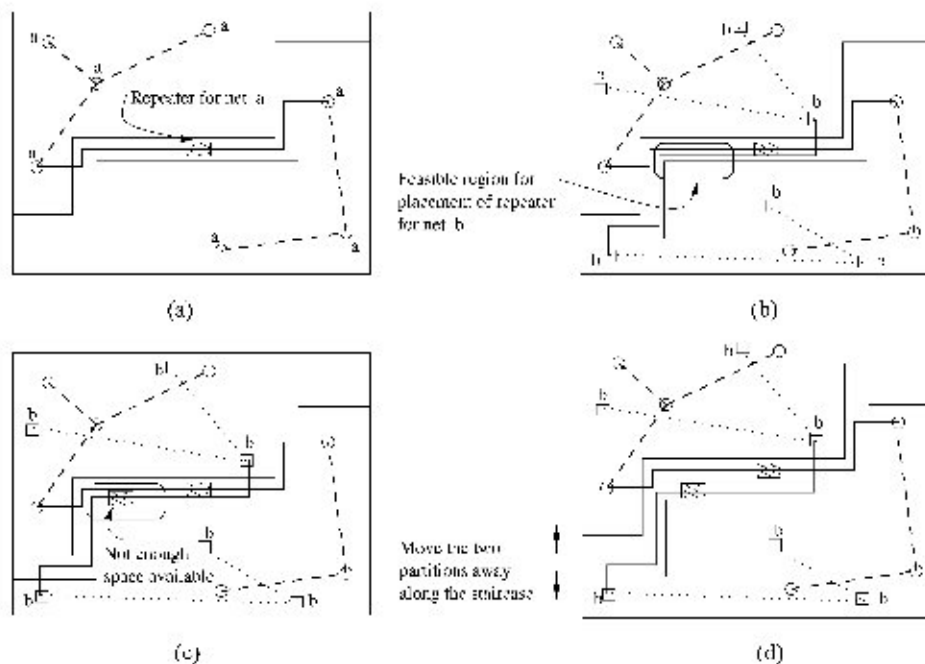


Fig. 3. A typical example of repeater placement.

2.2 Channel/Global Routing

The hierarchy involved in the *MSC* problem is useful for solving both channel and global routing. A floorplan is sliceable if it is obtained recursively by using through-cuts only. Hierarchical partitioning by the cut lines may be used to facilitate global routing. Nonsliceability of floorplans leads to infeasible channel routing order [Sur-Kolay and Bhattacharya 1991], so in a general floorplan either the width of certain channels are overestimated, or multiple iterations of detailed routing are performed. In the former case, the wasted area in the chip may increase, and hence a minimal set of channels needs to be chosen for widening, whereas the latter option requires more CPU time.

If, on the other hand, the routing region is generalized to a monotone staircase, the routing order is always acyclic, and can be easily obtained by identifying staircase channels hierarchically [Sur-Kolay and Bhattacharya 1991]. A monotone channel also guarantees a feasible routing order and can be widened easily, whereas for a nonmonotone channel, stretching routing regions along the x - or y -axis by simply moving the two parts away may not always help. In addition, this may require rip-up and reroute. Thus, the solution of the *MSC* problem offers a very good solution to channel routing. Efficient algorithms for routing through staircase channels using the manhattan-diagonal wiring model are available [Das et al. 2004]. Routing may be done in a single iteration without overestimation of the width for any channels. A related problem of finding the widest staircase channel among a set of isothetic obstacles can be solved in $O(n^2)$ time [Nandy and Bhattacharya 2003], where n is the number of

vertices of all the obstacles placed on the floorplan. This can be applied to the successful routing of a maximum number of nets. Needless to say, with five or six metal layers in the modern VLSI technology, channel routing may be mainly relevant in the device layers but the size of the problem is significant.

The *MSC* problem is also relevant to the global routing problem. The staircase channels separating the terminals are identified in a hierarchical manner, and then the nets in the hierarchy are routed in a bottom-up fashion. The nets crossing the staircases, which appear at the top of the hierarchy, are routed at the end, and hence should have less congestion in the corresponding portion of the metal layer. The nets in smaller partitions, which cross the staircases toward the bottom of the hierarchy, need only local routing and are easier to route. Therefore, the hierarchy of the *MSC* problem identifies an order for global routing. The rationale behind choosing a *minimal number of crossing nets* as one of the two optimization criteria is that the minimization of routing congestion is highly desirable in global routing.

3. PROBLEM FORMULATION

In our routing model, given a floorplan F with rectangular boundary and rectangular blocks, the routing region is the set of lines defining the boundary of the blocks. Our approach is to define a hierarchy of *ms-cuts* comprising of these lines. In the detailed routing step [Das et al. 2004], an *ms-cut* acquires finite width proportional to the number of tracks required for the nets assigned to it by the global router. With respect to staircase bipartitioning, a net is said to be *crossing* the staircase if it has terminals in both the partitions and the *cut-size* of the staircase is equal to the number of crossing nets. Let $n_l(n_r)$ and $A_l(A_r)$, respectively, denote the number and area of the blocks on the left (right) of the *ms-cut*.

Fact [Majumder 1996]: given a floorplan with n blocks, (i) the total number of possible *ms-cuts* is exponential, (ii) a hierarchy of *ms-cuts* always exists with exactly $n - 1$ *ms-cuts*.

Given F and its netlist, the following problems on *ms-cuts* may be formulated:

- Min-cut Problem* P_c [Majumder et al. 2004]: an *ms-cut* with minimum cut-size;
- Number-balance Problem* P_n [Dasgupta et al. 2002]: an *ms-cut* maximizing the number-balance ratio, $\frac{\min(n_l, n_r)}{\max(n_l, n_r)}$;
- Area-balance Problem* P_A : an *ms-cut* maximizing the area-balance ratio $\frac{\min(A_l, A_r)}{\max(A_l, A_r)}$.

Noting that problems P_c and P_n are polynomial time solvable, the two problems studied in this article are the mixed optimization problems concerning both balance and cut-size, namely, *Number-balanced Min-cut* P_{nc} and *Area-balanced Min-cut* P_{Ac} . The goal is to find an *ms-cut* maximizing the cost C which is a normalized convex combination of the respective balance-ratio and the cut-size. We, therefore define cost as $C = \gamma \cdot (\text{balance-ratio}) + (1 - \gamma) \cdot (1 - \text{cut-size} / \#\text{nets})$, $\gamma \in [0, 1]$.

The parameter γ is termed the *control factor*, which determines the tradeoff between balance-ratio of the bipartition and the cut-size. For $\gamma = 0$, the cost C is nothing but the min-cut; both P_{nc} and P_{Ac} reduce to P_c . Similarly, for $\gamma = 1$, the emphasis is on balance alone so the two problems reduce to P_n or P_A depending on the type of balance-ratio.

4. AREA-BALANCED MONOTONE STAIRCASE BIPARTITIONING

We prove that problem P_{Ac} is NP-hard by showing that problem P_A , the special case with $\gamma = 1$, is NP-hard. We actually consider the decision problem P'_A corresponding to P_A :

Definition 1. Area-balanced *ms-cut* (P'_A): does there exist an *ms-cut* in a given floorplan F such that $A_l = A_r$?

The convention is that all junctions in the floorplan are *T-junctions*, and a cross-junction is a pair of *T-junctions* with an infinitesimal skew. Starting from point P , the *bottom-left* corner of F , we move either upward or to the right. At each *T-junction* encountered, we choose nondeterministically either the $+x$ or $+y$ direction if both options exist, till we reach Q , the *top-right* corner. The path traversed is a *rising ms-cut*. The time taken is $O(n)$ as the number of operations is equal to the number of *T-junctions* visited, and the total number of *T-junctions* in F is $2n - 2$ [Sur-Kolay 1991]. Further, given an *ms-cut*, we can check in $O(n)$ time whether $A_l = A_r$. Hence $P'_A \in \text{NP}$. A polynomial reduction of the Set Partitioning Problem, which is known to be NP-complete [Garey and Johnson 1979], to P'_A is established next.

Definition 2. Set Partitioning Problem (SPP): given a finite set A and a size $s(a) \in \mathbb{Z}^+$ for each $a \in A$, does there exist a subset $A' \subseteq A$ such that $\sum_{a \in A'} s(a) = \sum_{a \in A - A'} s(a)$?

Given a set $A = \{a_1, a_2, \dots, a_k\}$, we construct an equivalent instance of the problem P'_A in three stages. First, we place a set $S = \{b_1, b_2, \dots, b_k\}$ of square blocks along the diagonal of a square floorplan (Figure 4(a)), where, for each $a_i \in A$, the area of block b_i is $s(a_i)$, and its side is of length $l_i = \sqrt{s(a_i)}$. In order to cover the entire floorplan, we place a set $B_{adj} = \bigcup_{i=1}^{k-1} \{b_{iL}, b_{iR}\}$ of $k - 1$ pairs of additional rectangular blocks (fillers) in the floorplan. As the shapes of all blocks b_i are square, the width $w(b_{iL})$ (along x -axis) is equal to the height $h(b_{iR})$, which in turn is l_i . It is also evident that the height $h(b_{iL})$ is equal to the width $w(b_{iR})$; thus $\text{Area}(b_{iL}) = \text{Area}(b_{iR})$ for $1 \leq i \leq k - 1$.

For any rising *ms-cut*, there is a corresponding partition of the set A . We need to find the *area-balanced ms-cut* for which the difference in the weight of the two corresponding partitions of A is zero. This correspondence holds if and only if the *ms-cut* passes through the point R_1 in Figure 4(a), because in that case, for all $i \in \{1, 2, \dots, k - 1\}$, b_{iL} and b_{iR} , respectively, belong to the left and right partitions and hence $\sum_{a_i \in A'} \text{Area}(b_{iL}) = \sum_{a_j \in A - A'} \text{Area}(b_{jR})$, thus ascertaining that the additional filler blocks cannot bias any partition.

In the second stage (Figure 4(b)), we ensure that the *area-balanced ms-cut* passes through R_1 by placing two more square blocks S_1 and S_2 along the

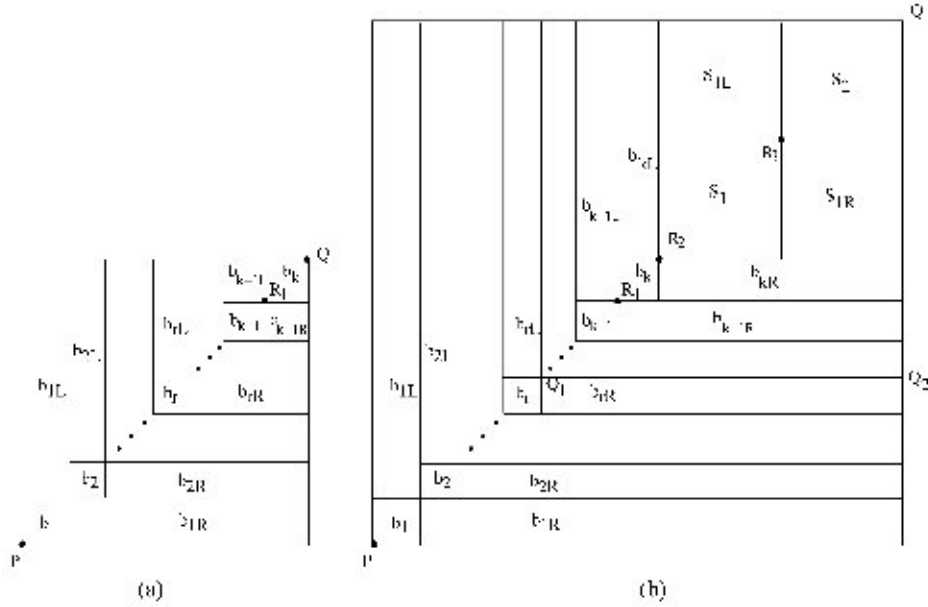


Fig. 4. Constructing an instance of a floorplan equivalent to a given instance of SPP: (a) first stage, (b) second stage.

diagonal of F such that $\text{Area}(S_1) = \text{Area}(S_2) = K' > K = \sum_{a_i \in A} s(a_i)$. The desired rectangular floorplan F is obtained by adding four more rectangular blocks b_{kL} , b_{kR} , S_{1L} , and S_{1R} , as shown in Figure 4(b).

LEMMA 1. *For an area-balanced ms -cut χ in F , the blocks S_1 and S_2 cannot both be in the same partition.*

PROOF. Suppose an area-balanced ms -cut χ passes through the points Q_1 and Q_2 (Figure 4(b)) keeping both S_1 and S_2 in its left partition. Even if all the blocks b_1, b_2, \dots, b_r lie in the right partition, the difference in area between the two partitions is $|A_l - A_r| \geq 2K' - K > K'$, which is a contradiction. On the contrary, for any ms -cut that keeps blocks S_1 and S_2 in different partitions, we have $|A_l - A_r| \leq K < K'$. This is certainly true if χ is an Area-balanced ms -cut and $|A_l - A_r| = 0$. Such an ms -cut has to pass through the points R_1, R_2 and R_3 , keeping S_1 and S_2 on either side. \square

The above lemma shows that, for an *area-balanced ms -cut*, the additional blocks do not bias the area of either partition. Finally, we replace the cross-junctions with T -junctions in the floorplan F , such that neither of the partitions gets biased in this process. As shown in Figure 5, the same nonzero skew of d is introduced at each cross-junction by (i) increasing the height of S_{1R} and each b_{iR} block by $d/2$, and (ii) introducing another k pairs of additional rectangular blocks b_{iL}^* and b_{iR}^* , for $1 \leq i \leq k$, and S_{1L}^* and S_{1R}^* with the following dimensions:

$$\begin{aligned} w(b_{iR}^*) &= w(b_{iR}) - d \text{ and } h(b_{iR}^*) = d/2; \\ w(S_{1R}^*) &= w(S_{1R}) - d \text{ and } h(S_{1R}^*) = d/2; \end{aligned}$$

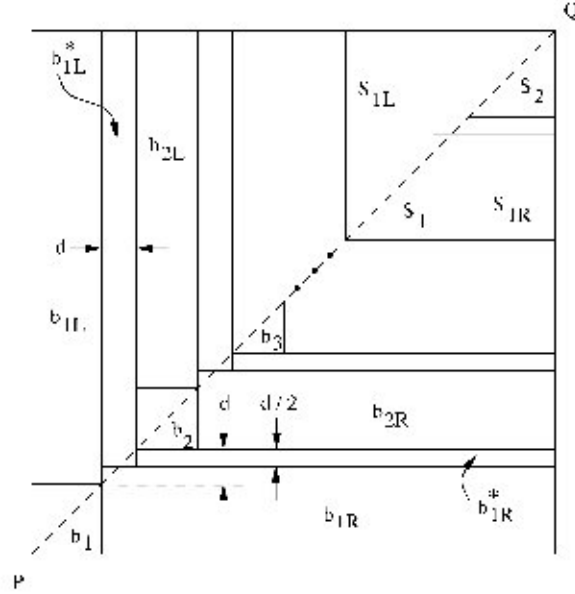


Fig. 5. Final stage in the reduction of SPP to area-balanced *ms-cut* in a floorplan F : removal of cross-junctions.

$$\begin{aligned} w(b_{1L}^*) &= d \text{ and } h(b_{1L}^*) = h(b_{1L}) - d/2; \\ w(S_{1L}^*) &= d \text{ and } h(S_{1L}^*) = h(S_{1L}) - d/2. \end{aligned}$$

Now for any i , while the introduction of the block b_{iR}^* leads to an increase in area of the right partition and $b_{iR} > b_{iL}$, the increase in area of the left partition is due to the block b_{iL}^* . The square shape of the floorplan F is, however, preserved.

Let the length of each side of F be L . Then considering the cross-junction between blocks b_1 and b_2 :

$$\begin{aligned} \text{Area}(b_{1R}) - \text{Area}(b_{1L}) &= (L - l_1) \cdot d/2, \\ \text{Area}(b_{1R}^*) &= (L - l_1 - d) \cdot d/2, \text{ and } \text{Area}(b_{1L}^*) = d \cdot (L - l_1 - d/2). \end{aligned}$$

In other words,

$$\begin{aligned} &(\text{Area}(b_{1R}) - \text{Area}(b_{1L})) + \text{Area}(b_{1R}^*) \\ &= (L - l_1) \cdot d/2 + (L - l_1 - d) \cdot d/2 \\ &= (2L - 2l_1 - d) \cdot d/2 \\ &= (L - l_1 - d/2) \cdot d \\ &= \text{Area}(b_{1L}^*). \end{aligned}$$

Therefore, $\text{Area}(b_{1R}) + \text{Area}(b_{1R}^*) = \text{Area}(b_{1L}) + \text{Area}(b_{1L}^*)$. For any i , we can show similarly that the above method of replacing cross-junctions between b_i and b_{i+1} does not bias the area of either of the partitions, irrespective of the value of d .

Hence, an *area-balanced ms-cut* in F corresponds exactly to a solution of SPP for set A . The time required to construct such an instance of the floorplan is $O(|A|)$ which is linear. From the above construction, we have the following theorem:

THEOREM 1. *Problem P'_A is NP-complete.*

PROOF. Consider an *area-balanced monotone staircase* in the floorplan constructed as above. This corresponds to the partitioning of A for which the difference in the sum of integers in the two partitions is zero and vice versa. The time required to construct such an instance of the floorplan is $O(|A|)$. Hence P'_A is NP-hard and as we already have $P'_A \in \text{NP}$, P'_A is NP-complete. \square

5. HEURISTIC FOR MIXED OPTIMIZATION

The NP-hardness of problem P_{Ac} mandates the design of an efficient heuristic for solving it. At this juncture, we also conjecture the following:

CONJECTURE 1. *Problem P_{nc} is NP-hard.*

For the problems P_{nc} and P_{Ac} , a common heuristic framework is therefore proposed. An instance of P_{Ac} with unit area blocks is equivalent to an instance of P_{nc} . As we require a balanced *ms-cut*, we construct a graph, similar to that for problem P_c [Majumder et al. 2004], and we apply a maxflow-based balanced bipartitioning method [Yang and Wong 1996].

5.1 Monotone Staircases

Given a floorplan F with the set of n blocks $B = \{b_i, |1 \leq i \leq n\}$ and netlist N , the adjacency digraph $G = (V, E)$ has a node v_i for each block b_i and an arc e_{ij} from v_i to v_j if block b_i is either to the top or left of b_j . The nodes for the two blocks at the top-left and bottom-right corners of F are designated as source s and sink t , respectively. Next, G is augmented as below to a digraph $G_{aug} = (V_{aug}, E_{aug})$ so that multiterminal nets are also represented.

5.1.1 Graph Augmentation. For each net $\eta_\alpha \in N$, let V^α be the set of nodes in V_{aug} corresponding to the set of blocks having terminals of the net η_α . We add two additional nodes s_α and t_α in V_{aug} , and call them *pseudosource* and *pseudosink*, respectively for the net η_α . Thus the augmented set of nodes is $V_{aug} = V \cup_{\eta_\alpha \in N} s_\alpha \cup_{\eta_\alpha \in N} t_\alpha$ with $|V_{aug}| = n + 2k$, k being the number of distinct nets. The set of arcs \bar{E}_{aug} comprises the following:

- a set of arcs $e_{st}(\alpha)$ (dashed lines in Figure 6);
- for each net η_α , we add three sets of new arcs:
 - $E_s(\alpha) = \{(v_i, s_\alpha) | v_i \in V^\alpha\}$,
 - $E_t(\alpha) = \{(t_\alpha, v_i) | v_i \in V^\alpha\}$,
 - an arc $e_{st}(\alpha)$ from s_α to t_α .

Thus $E_{aug} = \bar{E} \cup_{\eta_\alpha \in N} (E_s(\alpha) \cup E_t(\alpha), e_{st}(\alpha))$. The total number of arcs in E_{aug} is $O(n + k + t) = O(t)$, t being the number of terminals. The *capacity* of the edges $e_{st}(\alpha)$ is set to 1 and that of all other arcs in E_{aug} to ∞ . Figure 6 shows a typical G_{aug} with three nets a , c , and d .

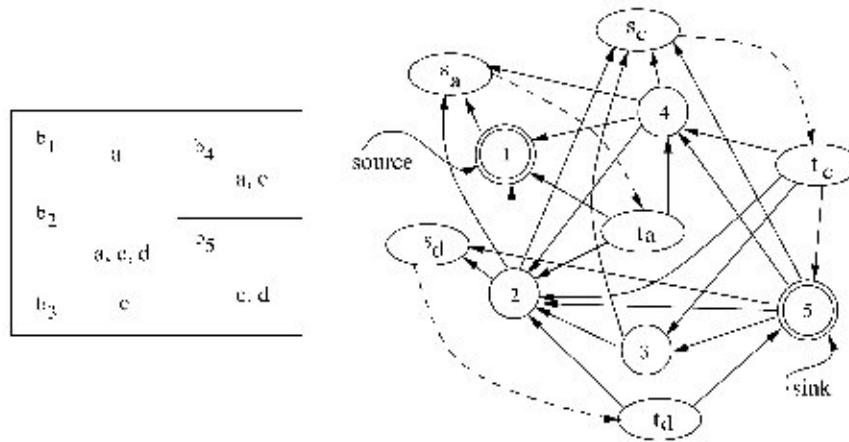


Fig. 6. Construction of G_{aug} with node 1 as source s and node 5 as sink t .

The methodology for the mixed optimization problems P_{Ac} and P_{nc} is based on Theorem 2 below, proven in Majumder et al. [2004]. A *monotone st-cut* in G_{aug} is a cut [Papadimitriou and Steiglitz 1982] in the graph that partitions the set of nodes V_{aug} in two sets S (*left partition*), and T (*right partition*), such that $s \in S$ and $t \in T$, and the arcs crossing the cut having infinite capacity are directed from T to S . For a monotone *st-cut* in G_{aug} , a net η_α contributes unit cost only if the blocks with net η_α are present on either side of the corresponding monotone staircase.

THEOREM 2. *A mincut in G_{aug} is a monotone st-cut of minimum cost and corresponds to the monotone staircase in the floorplan crossed by the minimum number of distinct nets.*

5.2 Flow-Based Balanced Bipartitioning

Given a network having weights associated with its nodes, a bipartition is said to be balanced if the weights of the two parts are each equal to $W/2$, where W is the sum of the weights associated with all its nodes. The key idea is to improve the balance ratio of a bipartition incrementally by determining the mincut [King et al. 1995] on the given network, then collapsing all nodes in the smaller partition with a randomly chosen node of the other part, and finding the mincut for the collapsed network. This can be implemented efficiently by computing the flow in the collapsed network incrementally instead of starting the maxflow algorithm all over again. The algorithm terminates when the weight of the left partition lies between $(1 - \epsilon)W/2$ and $(1 + \epsilon)W/2$, where the deviation factor $\epsilon < 1$ is chosen to be very small. It has been proved [Yang and Wong 1996] that the number of iterations and the final cut-size are nonincreasing functions of ϵ .

5.3 Overview of Heuristic

We describe below the plan of the heuristic for solving problems P_{nc} and P_{Ac}

Table I. Details of MCNC
Floorplan Benchmarks

Name	# Blocks	# Nets
apte	9	97
xerox	10	208
hp	11	83
ami33	33	123
ami49	49	408

function $MOP(F, \gamma, btype, \epsilon)$

Input: (i) A floorplan F with its netlist N , (ii) control factor γ ,
(iii) type of balance $btype$, and (iv) deviation factor ϵ .

Output: An ms -cut that satisfies the balance criterion
as well as maximizes the convex cost C (as defined in Sec. 3).

- Step 1.* Construct G_{aug} for given F ; initialize list L to ϕ .
repeat
Step 2. Find a mincut χ' using maxflow algorithm on G_{aug} .
Step 3. Compute balance-ratio depending on $btype$.
Step 4. Store χ' and its cost in L ; update G_{aug} by collapsing all nodes in its
smaller part corresponding to χ' to a node randomly chosen from the
other part, adjacent to χ' , to form the new source or sink accordingly.
until
cut χ' yields balanced bipartition of G_{aug} .
Step 5. return the cut in L with maximum cost.

The cut thus found yields two subgraphs of G_{aug} , and, with minor adjustments for definition of source and sink, the above function MOP can be called again. Thus a balanced hierarchy of ms -cuts is obtained by recursively calling MOP on each of the two subgraphs obtained, till the floorplans corresponding to the subgraphs have no nondegenerate staircases. The main algorithm *Staircase Hierarchy* is given below.

Algorithm Staircase Hierarchy

Input: A graph G_{aug} corresponding to given floorplan F .

Output: A tree of monotone staircases S_G .

- Step 1.* If F has more than three blocks and at least one valid staircase exists,
then $\chi := MOP(F, \gamma, btype, \epsilon)$ else return NULL.
Step 2. Determine s_G , the ms -cut in F corresponding to χ ,
producing the two subfloorplans F_L and F_R .
Step 3. $S_L := Staircase_hierarchy(F_L)$
Step 4. $S_R := Staircase_hierarchy(F_R)$
Step 5. return staircase tree S_G with root s_G , and
 S_L and S_R respectively as the left and right subtree of s_G .

6. EXPERIMENTAL RESULTS

We have implemented the heuristic for the mixed optimization problem and have run it on the five MCNC floorplan benchmarks given in Table I. We have been able to generate the hierarchy of ms -cuts in each case. Further, the effect of the control factor γ on the tradeoff between number of nets crossing ms -cut and the balance-ratio is evident from the results presented below.

Table II. Number-Balanced Staircase Hierarchies of *ami33* for Various Balance-Ratios

Cut #	# Blk.	# Nets	Bal. ratio	Net cut	Cost C	Cut #	# Blk.	# Nets	Bal. ratio	Net cut	Cost C
$\gamma = 0$						$\gamma = 0.2$					
1	33	80	1/32	5	0.94	1	33	80	1/32	5	0.76
2	32	79	1/31	2	0.98	2	32	79	1/31	2	0.79
3	31	79	1/30	7	0.91	3	31	79	1/30	7	0.74
4	30	76	1/29	5	0.93	4	30	76	1/29	5	0.75
5	29	74	1/28	8	0.89	5	29	74	1/28	8	0.72
6	28	72	1/27	5	0.93	6	28	72	1/27	5	0.75
7	27	71	1/26	12	0.83	7	27	71	6/21	13	0.71
8	26	65	1/25	7	0.89	8a	6	12	3/3	7	0.53
9	25	64	1/24	4	0.94	8b	21	58	1/20	7	0.71
10	24	64	1/23	5	0.92	9	20	55	1/19	6	0.72
11	23	61	1/22	7	0.89	10	19	54	1/18	7	0.71
12	22	60	1/21	7	0.88	11	18	51	2/16	7	0.72
13	21	57	1/20	8	0.86	12	16	47	1/15	8	0.68
14	20	55	1/19	7	0.87	13	15	44	1/14	6	0.71
15	19	52	1/18	6	0.89	14	14	40	3/11	7	0.72
16	18	51	1/17	8	0.84	15	11	34	3/8	6	0.73
17	17	48	2/15	7	0.85	16	8	32	1/7	5	0.70
18	15	44	2/13	6	0.86	17	7	31	3/4	6	0.80
19	13	38	1/12	6	0.84	18	4	25	1/3	16	0.36
20	12	34	1/11	3	0.91						
21	11	34	2/9	5	0.85						
22	9	33	1/8	5	0.85						
23	8	32	1/7	5	0.84						
24	7	31	1/6	16	0.48						
25	6	15	2/4	3	0.80						
26	4	10	2/2	7	0.30						
$\gamma = 0.4$						$\gamma = 0.6$					
1	33	80	9/24	21	0.59	1	33	80	13/20	37	0.61
2a	24	61	11/13	21	0.73	2a	13	18	5/8	12	0.51
3a	11	16	2/9	4	0.54	2b	20	46	8/12	18	0.64
3b	13	35	3/10	6	0.62	3a	8	12	4/4	9	0.70
4a	9	16	4/5	8	0.62	3b	12	24	5/7	8	0.69
4b	10	33	3/7	9	0.61	4a	4	4	2/2	4	0.60
5	4	8	2/2	8	0.40	4b	5	20	2/3	18	0.44
$\gamma = 0.8$						$\gamma = 1.0$					
1	33	80	13/20	37	0.63	1	33	80	13/20	37	0.65
2a	13	18	5/8	12	0.57	2a	13	18	5/8	12	0.63
2b	20	46	8/12	18	0.66	2b	20	46	8/12	18	0.67
3a	8	12	4/4	9	0.85	3a	8	12	4/4	9	1.00
3b	12	24	5/7	8	0.71	3b	12	24	5/7	8	0.71
4a	4	4	2/2	4	0.80	4a	4	4	2/2	4	1.00
4b	5	20	2/3	18	0.55	4b	5	20	2/3	18	0.67

As a typical case, we present the results of the entire run of our proposed heuristic on floorplan *ami33* in Tables II and III for number-balance and area-balance, respectively. For brevity, we have omitted the detailed tables for the other benchmark floorplans but the outcome of our experiments is presented in a comprehensive manner in the plots shown in Figure 7. Finally, Table IV gives an idea about the time taken by our heuristic.

Table III. Area-Balanced Staircase Hierarchies of *ami33* for Various Balance-Ratios

Ct. #	B	N	Num. rat.	Area rat.	Ct. sz.	C	Ct. #	B	N	Num. rat.	Area rat.	Ct. sz.	C
$\gamma = 0$							$\gamma = 0.2$						
1	33	80	1/32	0.022	5	0.94	1	33	80	1/32	0.022	5	0.75
2	32	79	1/31	0.011	2	0.98	2	32	79	1/31	0.011	2	0.78
3	31	79	1/30	0.005	7	0.91	3	31	79	1/30	0.005	7	0.73
4	30	76	1/29	0.077	5	0.93	4	30	76	1/29	0.077	5	0.76
5	29	74	1/28	0.035	8	0.89	5	29	74	1/28	0.035	8	0.72
6	28	72	1/27	0.015	5	0.93	6	28	72	1/27	0.015	5	0.75
7	27	71	1/26	0.040	12	0.83	7	27	71	6/21	0.304	13	0.71
8	26	65	1/25	0.019	7	0.89	8a	6	12	3/3	0.447	7	0.42
9	25	64	1/24	0.046	4	0.94	8b	21	58	1/20	0.079	7	0.72
10	24	64	1/23	0.013	5	0.92	9	20	55	1/19	0.068	6	0.73
11	23	61	1/22	0.027	7	0.89	10	19	54	1/18	0.023	7	0.70
12	22	60	1/21	0.069	7	0.88	11	18	51	2/16	0.038	7	0.70
13	21	57	1/20	0.137	8	0.86	12	16	47	1/15	0.033	8	0.67
14	20	55	1/19	0.021	7	0.87	13	15	44	1/14	0.013	6	0.69
15	19	52	1/18	0.069	6	0.89	14	14	40	2/12	0.143	6	0.71
16	18	51	1/17	0.031	8	0.84	15	12	34	3/9	0.865	6	0.83
17	17	48	2/15	0.039	7	0.85	16	9	32	1/8	0.166	3	0.76
18	15	44	2/13	0.140	6	0.86	17	8	32	4/4	0.662	7	0.76
19	13	38	1/12	0.015	6	0.84	18	4	25	1/3	0.593	16	0.41
20	12	34	1/11	0.082	3	0.91							
21	11	34	2/9	0.640	5	0.85							
22	9	33	1/8	0.113	5	0.85							
23	8	32	1/7	0.255	5	0.84							
24	7	31	1/6	0.343	16	0.48							
25	6	15	2/4	0.804	3	0.80							
26	4	10	2/2	0.021	7	0.30							
$\gamma = 0.4$							$\gamma = 0.6$						
1	33	80	13/20	0.696	37	0.60	1	33	80	13/20	0.696	37	0.63
2a	13	18	1/12	0.202	3	0.58	2a	13	18	6/7	0.792	13	0.59
2b	20	46	8/12	0.682	22	0.59	2b	20	46	8/12	0.682	22	0.62
3a	12	16	4/8	0.966	10	0.61	3a	7	6	3/4	0.919	2	0.82
3b	8	19	3/5	0.695	4	0.75	3b	6	6	2/4	0.555	2	0.60
4a	4	7	1/3	0.990	7	0.40	3c	8	19	3/5	0.695	4	0.73
4b	8	4	3/5	0.943	3	0.53	4	5	19	2/3	0.798	18	0.50
4c	5	19	1/4	0.482	14	0.35							
$\gamma = 0.8$							$\gamma = 1.0$						
1	33	80	13/20	0.696	37	0.66	1	33	80	13/20	0.696	37	0.70
2a	13	18	6/7	0.792	13	0.69	2a	13	18	6/7	0.792	13	0.79
2b	20	46	8/12	0.682	22	0.65	2b	20	46	8/12	0.682	22	0.68
3a	7	6	3/4	0.919	2	0.87	3a	7	6	3/4	0.919	2	0.92
3b	6	6	3/3	0.703	4	0.63	3b	6	6	3/3	0.703	4	0.70
3c	8	19	3/5	0.695	4	0.71	3c	8	19	3/5	0.695	4	0.69
4	5	19	2/3	0.798	18	0.65	4	5	19	2/3	0.798	18	0.80

We have tested for six values of γ on each of the benchmarks. One of the important goals of these experiments is to determine a suitable value of γ , which can then be used for other floorplans. In Table II, γ is varied from 0 to 1 in increments of 0.2; recall that $\gamma = 0$ corresponds to minimum cut-size without balance, and $\gamma = 1$ to balanced bipartition. The values of γ lying between 0 and

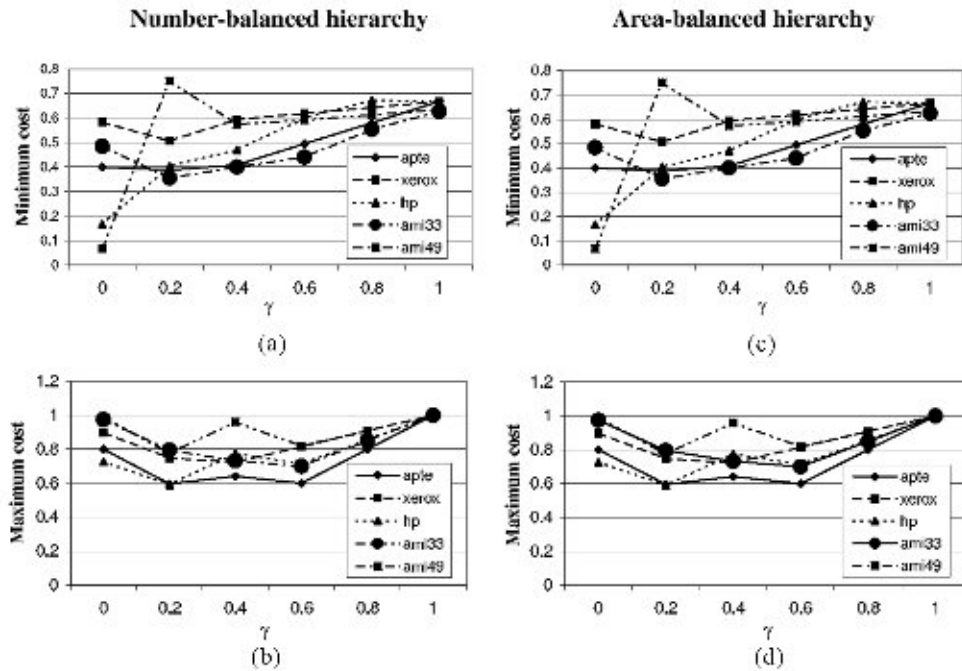


Fig. 7. Effect of γ on minimum and maximum values of cost over all levels of number-balanced and area-balanced hierarchies of *ms-cuts*.

1 lead to the mixed optimization problem. For each value of γ , the first column *Cut #* gives the depth of the hierarchy of the cuts generated. When $\gamma = 0$, the cuts generated are highly unbalanced and at each level we have only one staircase. But for $\gamma > 0$, each level in the hierarchy except the first has more than one *ms-cuts*, for example, level 2 has two *ms-cuts* 2a and 2b. The next two columns give the number of blocks and nets being partitioned by the *ms-cut* at that node of the hierarchy. Column *Bal.-ratio* gives the number of blocks on left/right sides of the cut. Column *Net cut* gives the number of nets crossing the cut and Column *Cost* has C , the cost of mixed optimization.

Table III is similar to Table II, with the fourth column renamed as *Num. rat.* followed by an additional column *Area rat.*, where the balance of areas of the two partitions generated by each *ms-cut* is also shown. In both these tables, the following facts are observed quite naturally. With an increase in γ , the balance factor increases, which in turn brings down the number of levels of hierarchy, whereas the number of nets crossing the cut increases. For interpreting the effect of tradeoff control parameter γ on the cost of mixed optimization, we have plotted the minimum and maximum cost over all levels for each of the benchmarks in Figure 7. No notable difference, as far as the minimum and maximum values of cost are concerned, was found between the number-balanced and area-balanced bipartitions. This signifies that the type of balance does not have a strong impact on optimization cost C . Further, for $\gamma \geq 0.4$, these values do not vary much. Hence, it may be inferred that employing the heuristic in that range of γ can produce satisfactory results.

Table IV. Variation of Number of Levels and Maximum Cut-size with γ

Bench- mark Name	γ	Number-Balanced Type			Area-Balanced Type		
		# Levels	Max Cut-size over all Levels	CPU Time (in sec)	# Levels	Max Cut-size over all Levels	CPU Time (in sec)
apte	0	6	13	0.020	6	13	0.010
	0.2	4	15	0.030	4	13	0.010
	0.4	2	28	0.020	2	28	0.020
	0.6	2	28	0.020	2	28	0.020
	0.8	2	28	0.010	2	28	0.010
	1	2	28	0.010	2	28	0.010
xerox	0	7	61	0.050	7	61	0.040
	0.2	6	61	0.060	6	76	0.020
	0.4	2	81	0.050	3	81	0.020
	0.6	2	81	0.030	3	81	0.040
	0.8	2	81	0.020	3	81	0.020
	1	2	81	0.020	3	81	0.010
hp	0	8	16	0.020	8	16	0.020
	0.2	6	16	0.010	8	16	0.020
	0.4	4	30	0.010	4	23	0.020
	0.6	2	33	0.030	2	33	0.020
	0.8	2	33	0.010	2	33	0.030
	1	2	33	0.020	2	33	0.020
ami33	0	25	16	0.080	25	16	0.090
	0.2	18	16	0.180	18	16	0.130
	0.4	5	21	0.040	4	37	0.040
	0.6	4	37	0.040	4	37	0.060
	0.8	4	37	0.030	4	37	0.050
	1	4	37	0.050	4	37	0.050
ami49	0	43	25	0.440	43	25	0.470
	0.2	43	25	0.510	43	24	0.460
	0.4	5	173	0.280	5	192	0.150
	0.6	4	178	0.170	5	192	0.160
	0.8	4	178	0.130	5	192	0.160
	1	4	178	0.190	5	192	0.160

In Figure 8 we have focused on the *first level of the hierarchy* of cuts. This is the most computation-intensive level as well as the most important one as it affects the quality of the cuts in the subsequent levels also. For both number- and area-balanced type, we have plotted the balance-ratios (Figures 8(a) and 8(b)) and the cut-sizes (Figures 8(c) and 8(d)) at the first level for all the benchmarks. We find that for values of $\gamma \geq 0.4$ the balance factor becomes satisfactory as well as stable for both type of experiments. The cut-size, however, increases for the range $\gamma \geq 0.6$. So we can conclude that the most effective range is $0.4 \leq \gamma \leq 0.6$, when the tradeoff between cut-size and balance-ratio is optimal.

Finally, Table IV reports the number of levels versus the control factor γ . It also gives the maximum cut-size over all levels for different values of γ and the total CPU time taken to generate the hierarchy. The CPU time taken to partition the benchmarks is very low, as expected, as we have used a maxflow-based method, which is very fast. In Figure 9, the number of levels and maximum cut-size are plotted against γ . We find that the number of levels falls sharply (Figures 9(a) and 9(b)) around $\gamma = 0.4$ and then maintains the value up to

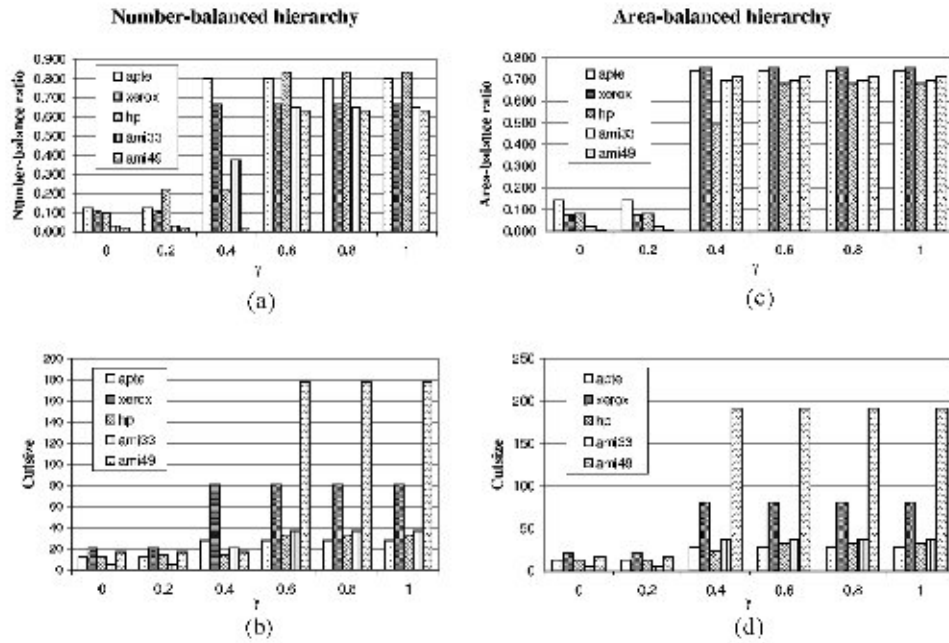


Fig. 8. Effect of γ on balance-ratio and cut-size in the first level of the staircase hierarchy.

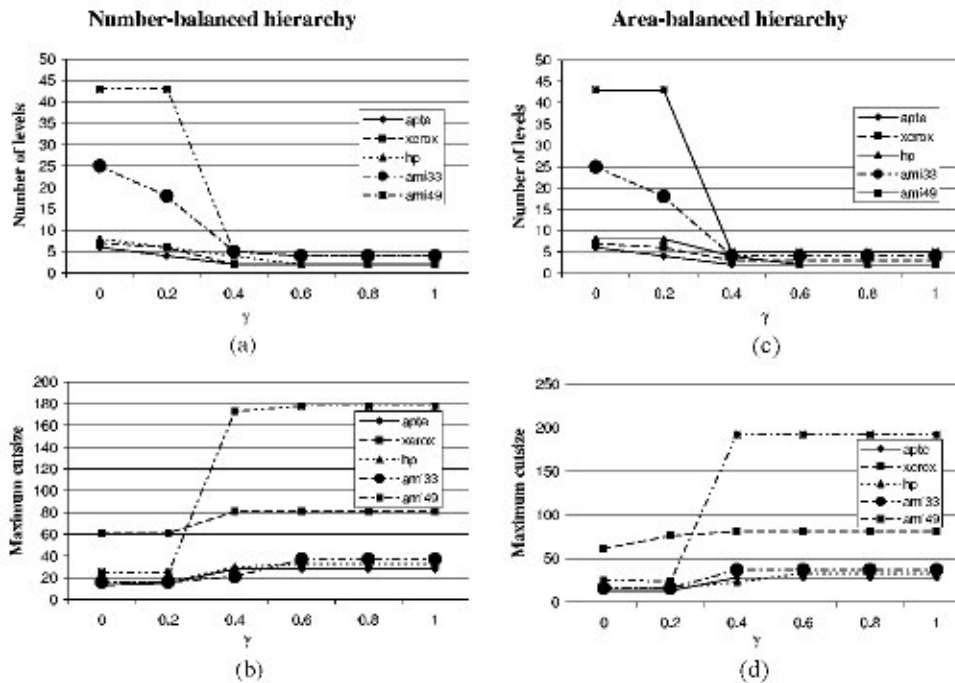


Fig. 9. Effect of γ on number of levels and maximum cut-size.

$\gamma = 1$. In order to keep the number of levels and, in turn, the CPU time, low, $\gamma = 0.4$ is a good engineering choice. Increasing γ further to increase the balance factor does not help much. In the other two plots (Figures 9(c) and 9(d)), the maximum cut-size across all levels is plotted against γ and again the best choice is $\gamma \leq 0.4$.

7. CONCLUSION

This article proposes a methodology for identifying a balanced hierarchy of monotone staircases with minimal cut-size in a VLSI floorplan. It is shown that the mixed optimization problem that balances area is NP-hard. A flow-based balanced bipartitioning method is designed to generate a hierarchy of monotone staircases which have as few nets crossing them as possible. Our experiments on the benchmark floorplans establish that mixed optimization of balance (number or area) and cut-size can be achieved efficiently. It has been found that the value of γ should preferably be chosen around 0.4 to obtain satisfactory outcome on a wide range of test cases. This problem has potential applications to minimization of global routing congestion, or repeater placement in the device layer.

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REFERENCES

- BURMAN, S., CHEN, H., AND SHERWANI, N. 1991. Improved global routing using δ -geometry. In *Proceedings of the 29th Annual Allerton Conference on Communication, Computing, and Control*.
- CHANG, C.-C., CONG, J., PAN, Z., AND YUN, X. 2003. Multilevel global placement with congestion control. *IEEE Trans. Comput.-Aid. Des. Integrat. Circ. Syst.* 22, 4 (Apr.), 395–409.
- CHU, C. C. N. AND WONG, D. F. 1997. Closed form solution to simultaneous buffer insertion/sizing and wire sizing. In *Proceedings of the International Symposium on Physical Design*. 192–197.
- CONG, J. 1997. Challenges and opportunities for design innovations in nanometer technologies. In *Frontier in Semiconductor Research: A Collection of SRC Working Papers*. Semiconductor Research Corporation. http://www.src.org/prg_mgmt/frontier.dgw.
- CONG, J., HE, L., KOH, C. K., AND MADDEN, P. H. 1996. Performance optimization of VLSI interconnect layout. *Integration, VLSI J.* 21, 1–94.
- CONG, J., KONG, T., AND PAN, D. Z. 1999a. Buffer block planning for interconnect-driven floorplanning. In *IEEE/ACM Digest of Technical Papers, International Conference on Computer Aided Design (ICCAD)*. 358–363.
- CONG, J., KONG, T., AND PAN, D. Z. 1999b. Interconnect delay estimation models for synthesis and design planning. In *Proceedings of the Asia and South Pacific Design Automation Conference*. 97–100.
- DAS, S., SUR-KOLAY, S., AND BHATTACHARYA, B. B. 2004. Manhattan-diagonal routing in channels and switchboxes. *ACM Trans. Des. Automat. Electron. Syst.* 9, 1, 75–104.
- DASGUPTA, P. S., PAN, P., NANDY, S. C., AND BHATTACHARYA, B. B. 2002. Monotone bipartitioning problem in a planar point set with applications to VLSI. *ACM Trans. Des. Automat. Electron. Syst.* 7, 2, 231–248.
- GARRY, M. R. AND JOHNSON, D. S. 1979. *Computers and Intractability: A Guide to Theory of NP-Completeness*. W. H. Freeman and Co., New York, NY.

- GURUSWAMY, M. AND WONG, D. F. 1988. Channel routing order for building-block layout with rectilinear modules. In *IEEE/ACM Digest of Technical Papers, International Conference on Computer-Aided Design (ICCAD)*. 184–187.
- KING, V., RAO, S., AND TARJAN, R. E. 1995. A faster deterministic maxflow algorithm. *J. Algorithm.* 17, 3, 447–474.
- MAJUMDER, S. 1996. Routing driven floorplan partitioning using staircase channel. M.S. thesis. Indian Statistical Institute, Kolkata, India.
- MAJUMDER, S., NANDY, S. C., AND BHATTACHARYA, B. B. 2004. On finding a staircase channel with minimum crossing nets in a VLSI floorplan. *J. Circ. Syst. Comput.* 13, 5, 1019–1038.
- MAJUMDER, S., SUR-KOLAY, S., BHATTACHARYA, B. B., AND NANDY, S. C. 2001. Area(number)-balanced hierarchy of staircase channels with minimum crossing nets. In *Proceedings of the International Symposium on Circuits and Systems (ISCAS, Sydney, Australia)*. Vol. V. 395–398.
- NANDY, S. C. AND BHATTACHARYA, B. B. 2003. On finding an empty staircase polygon of largest area (width) in a planar point-set. *Computat. Geom. Theor. Appl.* 26, 143–171.
- OKAMOTO, T. AND CONG, J. 1996. Interconnect layout optimization by simultaneous steiner tree construction and buffer insertion. In *Proceedings of the ACM/SIGDA Physical Design Workshop*. 1–6.
- PAPADIMITRIOU, C. H. AND STEIGLITZ, K. 1982. *Combinatorial Optimization: Algorithms and Complexity*. Prentice Hall, Englewood Cliffs, NJ.
- SARKAR, P. AND KOH, C. K. 2001. Routability-driven repeater block planning for interconnect-centric floorplanning. *IEEE Trans. Comput.-Aid. Des. Integrat. Circ. Syst.* 20, 660–671.
- SHERWANI, N. 1993. *Algorithms for VLSI Physical Design Automation*. Kluwer Academic Publishers, Boston, MA.
- SUN, R., GUPTA, R., AND LIU, C. 1996. Congestion-balanced placement for FPGAs. In *Proceedings of the 5th Physical Design Workshop*. 163–168.
- SUR-KOLAY, S. 1991. Studies on nonslicible floorplans in VLSI layout design. PH.D thesis, Jadavpur University, Calcutta, India.
- SUR-KOLAY, S. AND BHATTACHARYA, B. B. 1991. The cycle structure of channel graphs in non-sliceable floorplans and a unified algorithm for feasible routing order. In *Proceedings of the International Conference on Computer Design (ICCD)*. IEEE Computer Society Press, Los Alamitos, CA, 524–529.
- YANG, H. H. AND WONG, D. F. 1996. Efficient network flow based min-cut balanced partitioning. *IEEE Trans. Comput.-Aid. Des. Integrat. Circ. Syst.* 15, 1533–1540.