Manhattan-Diagonal Routing in Channels and Switchboxes

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New techniques are presented for routing straight channels, L-channels, switchboxes, and staircase channels in a two-layer Manhattan-diagonal (MD) model with tracks in horizontal, vertical, and $\pm 45°$ directions. First, an $O(l.d)$ time algorithm is presented for routing a straight channel of length l and density d with no cyclic vertical constraints. It is shown that the number of tracks h used by the algorithm for routing multiterminal nets satisfies $d \leq h \leq (d + 1)$. Second, an output-sensitive algorithm is reported that can route a channel with cyclic vertical constraints in $O(l.h)$ time using h tracks, allowing overlapping of wire segments in two layers. Next, the routing problem for a multiterminal L-channel of length l and height h is solved by an $O(l.h)$ time algorithm. If no cyclic vertical constraints exist, its time complexity reduces to $O(l.d)$ where d is the density of the L-channel. Finally, the switchbox routing problem in the MD model is solved elegantly. These techniques, easily extendible to the routing of staircase channels, yield efficient solutions to detailed routing in general floorplans. Experimental results on benchmarks show significantly low via count and reduced wire length, thus establishing the superiority of MD routing to classical strategies. The proposed algorithms are also potentially useful for general non-Manhattan area routing and multichip modules (MCMs).

1. INTRODUCTION

Routing of nets is an essential step in layout design [Ohtsuki 1986; Pal 2000; Sherwani 1999]. While solving the area routing problem optimally is NP-hard [Ohtsuki 1986], a typical approach is to first decompose the routing area into a set of routing regions (channels), then to perform global routing of the nets through the channels, and finally to carry out detailed routing in each region [Ho et al. 1991; Yoshimura and Kuh 1982]. Given a netlist in a routing region, the typical objectives of a detailed router are to complete interconnection; minimize routing area, wirelength, number of vias, congestion, and crosstalk; and

maximize yield. The routing solution and design time depend on the routing model. Various grid-based models of channel routing exist depending on the number of available layers, the routing mode such as (Manhattan/knock-knee/nonisothetic), layer assignments (reserved/unreserved), and terminal behavior (fixed, movable, or interchangeable) [Sherwani 1999]. The Manhattan and the knock-knee models [Sarrafzadeh 1987] have been studied extensively in the past two decades. Some effort has been made to develop algorithms in nonisothetic geometries such as times square mode using $\pm 60°$ directions [Lodi et al. 1990] and the diagonal model using $\pm 45°$ wires [Chen 1987; Lodi et al. 1991]. Song [1992] presented an optimal knock-knee diagonal routing for L-channel with two-terminal nets only. In the Manhattan-diagonal (MD) model, which combines diagonal and Manhattan geometries, channel routers based on sorting were proposed by Chaudhary and Robinson [1991] and Yan [1999, 2000]. Another MD channel router was presented by Wang [1991] but the track count and via count for denser channels seem to be high and too many jogs are required.

In a recent technological development, it has been reported [Cataldo and Fuller 2001] that routing on-chip wires diagonally enables a reduction in wire length of 20% on average, as well as 10% improvement in chip performance, 20% decrease in power consumption, and thereby 30% more chips per wafer due to smaller size. Moreover, at extremely high frequencies, conventional Manhattan (orthogonal 90° routing) alone is likely to lead to unwanted parasitic effects causing signal degradation. Diagonal wires along with orthogonal wires have the potential to alleviate interconnect-delay problems. The proposed routing architecture, called X-architecture, has been employed for a complete Reduced Instruction Set Computer (RISC) processor design based on five metal layers, with the lower three being dominantly orthogonal, while the fourth and fifth layers make extensive use of diagonal wires in the $+45°$ and $-45°$ directions respectively. A long-time prejudice against non-Manhattan geometries has kept chip manufacturers from using 45° wires for several years. As the shortest distance between two points is a straight line and not a rectilinear path, a 45° wire eliminates a via that is otherwise required to connect the vertical and horizontal wire segments in nonoverlap reserved layer routing model; thus there is less interconnect capacitance and improved performance. Hence, the latest challenge is to redesign computer-aided design (CAD) tools for routing, as well as timing-driven floorplanning/placement with appropriate routing estimators, to exploit the benefits of Manhattan-diagonal wiring.

Apart from the channel routing problem, algorithms for the realistic problem of detailed routing within a general routing region are also required. Layout topology often imposes an order in which the detailed routing of the regions is to be completed, as the location of some of the terminals may depend on the routing in an adjacent region. Assuming that the blocks in a rectangular floorplan are also rectangular, slicible topologies can be represented by a binary tree, and postorder traversal of this tree provides a safe routing order [Dai et al. 1985], for example, $< 2, 3, 4, 1 >$ in Figure 1(a). Cyclic dependencies in routing order for nonslicible topologies (Figure 1(b)) can be overcome by introducing L-shaped routing regions (henceforth referred as L-channels as in
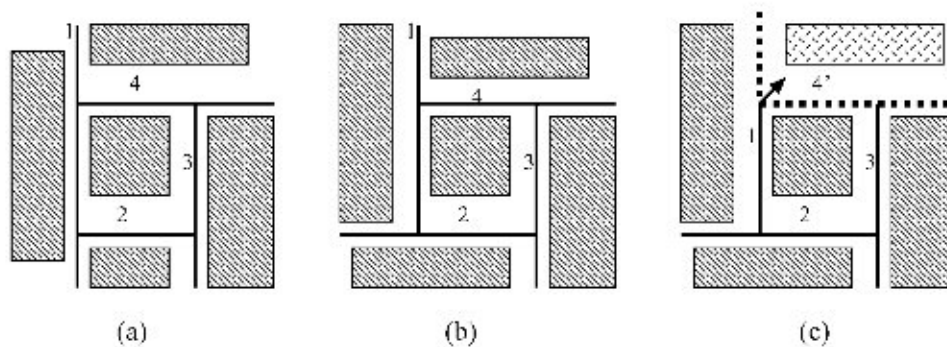
Fig. 1.   Safe routing order of channels.

Figure 1(a)) [Dai et al. 1985; Sur-Kolay and Bhattacharya 1991]. In Figure 1(c), the safe routing order is $< 1, 2, 3, 4' >$, where $4'$ is an L-channel. An L-channel can be further generalized to a monotone staircase channel [Guruswamy and Wong 1988; Majumder et al. 1998; Sur-Kolay and Bhattacharya 1991] that also guarantees safe routing order. The problem of safe ordering with minimum number of switchboxes has been solved efficiently [Yan and Hsiao 1996]. Even though the routing of a four-sided switchbox is a difficult problem in general, its importance is revived as it also arises in tower routing of MCMs [Sherwani 1999; Sherwani et al. 1995]. These issues motivate us to provide a unified strategy for solving the problem of routing L-channels, staircases, and switchboxes.

For a general junction, Maddila et al. [1989] proposed a routing method under the restrictive knock-knee model. Tsai et al. [1992] formulated general area routing as a planning problem decomposing the routing process into a conjunction of subgoals, each subgoal consisting of a selection of net segments and the assignment of track resources. However, it may need backtracking and may not report any solution as it uses the Manhattan model, even if a valid MD routing exists. The time complexity of this method is high. Thus, solving MD routing in general regions is also an open problem.

Section 2 summarizes the main results. In Section 3, preliminaries are discussed. The next two sections deal with channel routing algorithm in reserved and unreserved layer models respectively. Section 6 deals with L-channel routing. Next, in Section 7, switchbox routers in the MD-model for both reserved and unreserved layer models are proposed. These outperform existing routers; in particular, an extra row or column is not required to route Burstein's and other difficult benchmark switchboxes. Finally, a scheme for staircase channel routing is given in Section 7. Section 8 concludes the paper.

2. MAIN RESULTS

This paper outlines a new approach to detailed routing that combines the advantage of both the diagonal model and Manhattan geometry. We consider two routing layers with fixed terminals, and the Manhattan-diagonal ($\pm45°$) model. Thus, wire segments may either be rectilinear or at $\pm45°$ directions. Although there are several routing layers nowadays, typical routing strategies tackle signal routing from bottom to top layers taking two at a time. First, we consider

channel routing in the reserved layer model (i.e., the horizontal and diagonal wire segments in one layer and the vertical wire segment in the other layer), and present an $O(l.d)$ time algorithm that routes a channel with no cyclic vertical constraints in h tracks, where l is the length of the channel, d is the channel density, and $d \leq h \leq (d + 1)$. Berger et al. [1995] proposed an algorithm that routes any two-terminal net problem with density d using at most $d + O(\sqrt{d})$ tracks. For multiterminal nets, the upper bound on the usage of tracks is $2d + O(\sqrt{d})$. We show that if the vertical constraint graph of a multiterminal channel routing instance is acyclic, the upper bound on track usage for completion of the routing is $d + 1$.

Next, we describe an output-sensitive algorithm that can route channels with cyclic vertical constraints using h tracks, in $O(l.h)$ time (i.e., linear in the area of the channel), assuming an unreserved layer MD model where horizontal, vertical, and diagonal wire segments are in any layer that allows overlapping of wiring segments on two layers. The proposed algorithms outperform those reported earlier [Chaudhary and Robinson 1991; Ho et al. 1991; Pal et al. 1995; Yoshimura and Kuh 1982] both in time complexity and quality of solutions. Experiments with benchmark examples show very encouraging results. The router outputs an 18-track solution for the Deutsch's [1985] difficult example, a two-track solution for Burstein's difficult channel [Burstein and Pelavin 1983], and a 15-track solution for cycle.tough [Ho 1989] without inserting any extra row or column. The router also produces solutions with low via count and reduced wire length compared to the via minimizer of [The et al. 1991]. To the best of our knowledge, routing of these benchmarks in the MD model is being reported for the first time.

We also propose new algorithms for detailed routing of L-channels, switchboxes and staircases in the two-layer MD model. For L-channel routing, the core of the proposed method lies in routing a right-angled triangular region. This greedy heuristic method assumes a nonoverlap/reserved layer routing model, and can handle cyclic constraints. The complexity of all the algorithms presented are linear in the area of the region. These techniques can provide a unified and efficient routing paradigm to solve a general class of routing problems.

The design rules for the MD model as illustrated in Figure 2, can be supported by the CMOS fabrication process [Pucknell and Eshraghian 1996]. We recommend that the minimum separation rule between a via and a 45° wire, as in Figure 2(b), be made more robust by using octagonal vias (Figure 2(c)), other vias remaining square. Henceforth, a square (octagonal) via will be represented by a solid square (circle) in all subsequent figures.

3. PRELIMINARIES

A rectangular channel consists of two rows of terminals, placed along two of its parallel sides, on l (length) equidistant columns. The channel is called horizontal (vertical) depending on the direction of the parallel sides on which the terminals lie. An integer i, $0 \leq i \leq n$, is assigned to each terminal. All terminals with the same integer label i, $i \geq 1$ belong to the same net and are to be connected, while those labeled with 0 represent unconnected terminals.
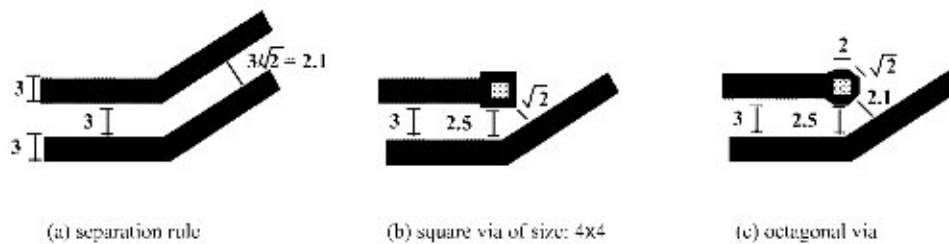
Fig. 2.   Design-rules in λ units for Manhattan-diagonal model.

The objective of the classical channel routing problem is to connect all the terminals specified by a given netlist with minimum number of tracks h (channel height [Sherwani 1999]), thus minimizing the channel area. Reducing via count and/or wire length is also important for high-performance layout design. The horizontal constraint graph (HCG) is an undirected graph whose nodes corresponds to nets, and there is an edge between node i and node j if along the channel the interval spanned by net i intersects that by net j. The density d of a channel is the maximum number of nets crossing a column in the channel, that is, the size of the max-clique in the horizontal constraint graph (HCG) [Pal 2000; Yoshimura and Kuh 1982]. The vertical constraint graph (VCG) is a directed graph whose nodes correspond to nets, and a directed edge from node i to node j exists if in any column, a terminal of net i appears on the top row and a terminal of net j on the bottom row. These two graphs play a major role in many channel routing algorithms. Routing of channels with cyclic vertical constraints often poses a difficulty and may need doglegging of nets in the reserved two-layer Manhattan model [Sherwani 1999].

An L-channel is an L-shaped rectilinear routing region comprising a vertical channel, and a horizontal channel with their respective bottom and left ends forming two adjacent sides of a rectangular region. This region at their meeting point is referred as the L-junction. Thus an L-channel is bounded by an external boundary, an internal boundary, and two open ends; it has no obstacles in its interior. It has equidistant terminals of nets along the external and internal boundaries. If it has l equidistant terminals on its external boundary, it is said to be of length l. The height h of an L-channel is said to be the greater of the heights of its vertical and horizontal channels. The objective is to connect the nets on an L-channel using minimum number of tracks. If extra tracks are required for completion of routing, the L-channel is expanded in the direction marked out as in Figure 1(c).

A switchbox is a rectangular routing region with terminals located on three or more sides. The region is said to consist of k rows and m columns. The objective is to obtain a valid connection of the nets within this region.

3.1 Design Rules for the MD Model

In the MD model, each layer of a channel C of length l and height h is assumed to consist of l × h grid points (Figure 3) formed by isothetic equidistant grid lines separated at a unit distance determined by the design rule. In addition, the diagonal tracks connect all pairs of grid points separated by a distance
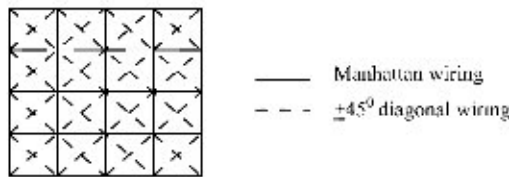
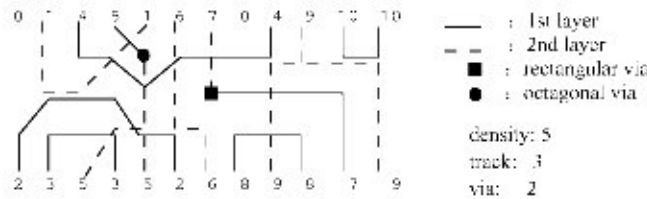Fig. 3.   Grid structure in Manhattan-diagonal (MD) model.

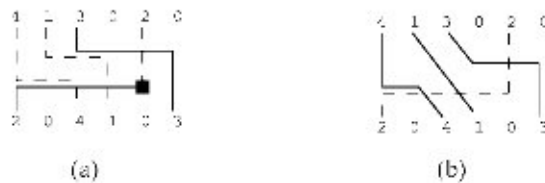Fig. 4.   Channel routing in unreserved layer MD model.

Fig. 5.   Illustration of lower bounds on h for a channel with density d = 4, in unreserved models: (a) h = 2 for Manhattan, (b) h = $\lceil(d - 2)/2\rceil$ = 1 for Manhattan-diagonal routing.

of $\sqrt{2}$. Thus, the degree of an interior node in the grid structure is 8. Terminals appear on the first and last rows of the channel, and vias must be placed on grid points.

3.2 Illustration of Area Efficiency of MD Model

Figure 4 shows a typical example [Yoshimura and Kuh 1982] of a rectangular channel which has been routed in an unreserved layer MD model. Only three tracks are used, whereas the channel density is 5.

3.3 Lower Bounds on the Number of Tracks in Channel Routing

In the reserved layer Manhattan model, it trivially follows from the definition of density of a channel that the minimum number of tracks h $\geq$ d. In the unreserved layer Manhattan model [Sherwani 1999], h $\geq \lceil d/2 \rceil$. The bound is further improved for the unreserved layer MD model, as observed below. Figure 5 shows comparative routing of an example. The lower bound (h = 1) can be achieved by slightly rerouting the net 3 in Figure 5(b).

OBSERVATION 1.   In the unreserved layer MD model, h $\geq \lceil(d - 2)/2\rceil$.

PROOF. As two different nets cannot pass through the same grid point of a given layer, at most 2h nets can be accommodated in a column in the Manhattan model. In the MD model, two extra nets may be routed through the same column
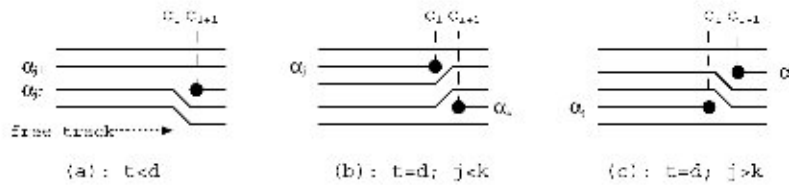
Fig. 6.   Transfer of nets onto adjacent tracks via diagonal edges.

(Figure 5(b)) using the diagonal edges between the top and bottom rows. So at most $2h + 2$ nets can pass through the column. Hence, $h \geq \lceil (d - 2)/2 \rceil$.   □

4. CHANNEL ROUTING IN THE RESERVED LAYER MD MODEL

4.1 Formulation

If the VCG is acyclic, then it is possible to route any arbitrary channel using a simpler MD model, with a reserved layer strategy. We assume that all horizontal and $\pm 45°$ wiring segments lie on one layer, and all vertical segments lie on the other layer. Thus, no two wire segments on two different layers overlap.

THEOREM 1.   A channel with density d and an acyclic VCG is routable in h tracks in the reserved layer MD model, where $d \leq h \leq d + 1$.

PROOF.   Since all the horizontal tracks lie in one layer, we have $h \geq d$. The rest of the proof follows from the following facts.

The vertices of the acyclic VCG are topologically ordered to yield a sequence of nets $S = \{a_1, a_2, \ldots, a_n\}$ such that if net a_i precedes net a_j in the VCG, then $j > i$. We now show that routing can be accomplished in at most $(d + 1)$ tracks such that the set of nets passing through any column, ordered from the topmost track to the bottom, is a subsequence of S.

Suppose routing is being done in the channel from left-to-right in a column-by-column fashion. Since $h \geq d$, we assume that at least d tracks are already laid out in the channel. Consider a column c_i where t tracks have already been occupied (Figure 6). The ordering of the nets occupying the tracks from top to bottom conforms with the sequence S. Tracks that are not assigned to any net in a column are called free in that column. We need to consider two cases.

Case 1:   Only one new net α_k begins (i.e., its leftmost terminal appears) at the next column c_{i+1}.

Case 1.1: $t < d$.
Assume that α_k appears between α_{j1} and α_{j2} ($j1 < j2$) in topological order. Then α_k can be accommodated using diagonal wiring within the interval (c_i, c_{i+1}) and a free track in c_{i+1} as shown in Figure 6(a). The sign of the diagonal (i.e., $+45°$ or $-45°$) depends on the relative position of the free track and the net α_k. Thus, column c_{i+1} needs at most d tracks.

Case 1.2: $t = d$.
Since t does not exceed d in any column, at least one net, say α_j (occupying track t_j) has to terminate at column c_i to make room for the incoming
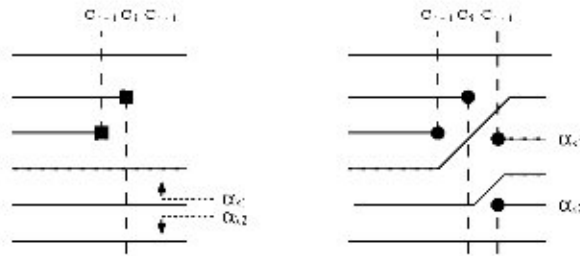
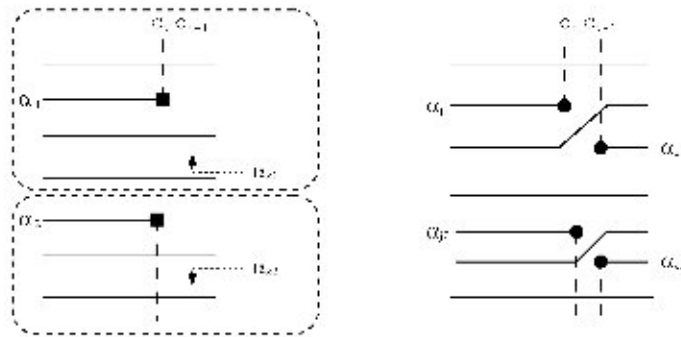Fig. 7. Accommodation of two incoming nets without inserting a track.

Fig. 8. Accommodation of two incoming nets in d tracks.

net in column c_{i+1}. If $k > j$ in net ordering (Figure 6(b)), then in column c_{i+1}, the net α_p is assigned to track t_{p-1} for all p, $j < p \leq k$. For other nets, track assignments are kept unchanged. Horizontal segments of the same net occupying adjacent tracks are then connected using $+45°$ diagonal wiring. If $k < j$, we need to use $-45°$ diagonals (Figure 6(c)). Thus, routing can be completed up to column c_{i+1} in d tracks preserving the net ordering in S.

Case 2:   Two new nets begin at column c_{i+1}.
  Let the two nets that begin at column c_{i+1} be α_{k1} and α_{k2} (let $k1 < k2$).

  Case 2.1:   Assume that at most $d - 1$ tracks are occupied in the previous column c_i, that is, at least one track is free. In addition, at least one net conforming to S, say α_{j1}, must terminate in column c_i. Using diagonal wiring from appropriate tracks in columns c_i and c_{i+1}, one can accommodate two incoming nets using at most d tracks as shown in Figure 7.

  Case 2.2:   Assume that d tracks are occupied in the previous column c_i; two nets, say α_{j1} and α_{j2} (let $j1 < j2$), must therefore terminate in column c_i. Assume with loss of generalitly that, $j1 < k1$.

  Case 2.2.1:   (i) $j1 < k1 < j2 < k2$; (ii) $j1 < k1 < k2 < j2$.
    Figure 8 shows Case 2.2.1(i). It is easy to see that the concerned portion of the channel can be partitioned horizontally into two parts, each of which encounters only one new net. From the results observed in Case 1,
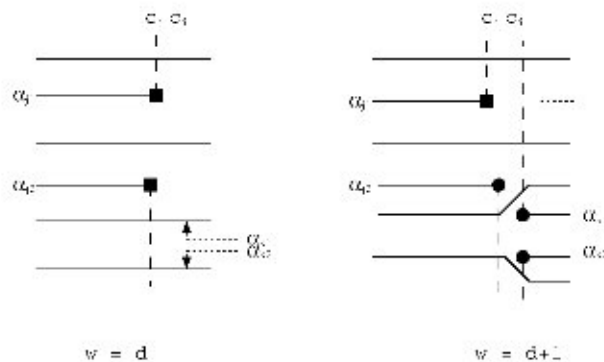
Fig. 9. An extra track is required to continue routing.

it follows that routing can progress from column c_i to c_{i+1} using only d tracks (Figure 8). Case 2.2.1(ii) is similar.

Case 2.2.2: $j1 < j2 < k1 < k2$.

Figure 9 illustrates this case, where one extra track is required to continue routing. Thus, $(d+1)$ tracks are necessary and sufficient in column c_{i+1}. Since the congestion of a column cannot exceed d, one track must be free in column c_{i+1}. Hence, for all subsequent columns, by virtue of Case 1 and Case 2.1, no more than $(d+1)$ tracks are required.

Since the VCG is acyclic, the order of the nets remains invariant throughout the length of the channel. Thus, the progressive routing strategy discussed above will be successful using h tracks, where $d \leq h \leq (d+1)$.   □

4.2 Algorithm 1: MD-CR (Reserved Layer MD Channel Router)

Input: A channel C of length l with columns $c_1, c_2, \ldots, c_l$ from left to right, a netlist of n nets (acyclic VCG), and two routing layers.

Output: Reserved layer MD routing (horizontal and $\pm 45°$ connections in one layer, and vertical connections in other layer), in at most $(d+1)$ tracks.

begin

Step 1. (a): Topologically sort the nodes of the acyclic VCG
                    and construct an ordered sequence of nets $\{a_1, a_2, \ldots, a_n\}$.
            (b): Determine the density d of C;
                    freetrack $(c_0) = d$; /* d free tracks in C */;

Step 2. Assign track 1 and track d respectively to the nets corresponding to the terminals on top and bottom in column c_1;
            $i := 2$;

Step 3. Repeat
            (a)   if leftmost or rightmost terminal of any net does not appear in column c_i
                    then track assignment for column c_i is same as in column c_{i-1};
            (b)   if r nets ($r = 1$ or 2) terminate in column c_i then mark the free tracks;
                    freetrack(c_i) := freetrack(c_{i-1}) + r;
            (c)   #new-net(c_i) = 1 then /* freetrack(c_{i-1}) ≥ 1 */
                    locate track t_j that fits the incoming net satisfying the topological order;
                    if track is not free then make it free by using diagonal connections
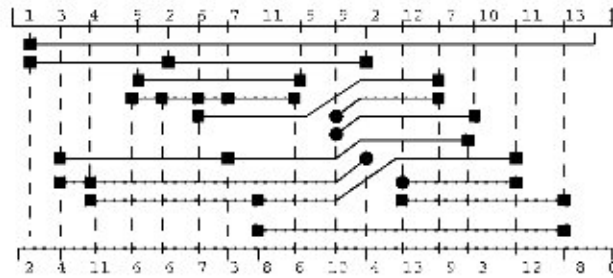   from the grid points in column c_{i-1} and assign the tracks in column c_i

Fig. 10.   An example of reserved layer MD routing with density $d = 9$, $v_{max} = 13$, and the number of tracks $h = 10$.
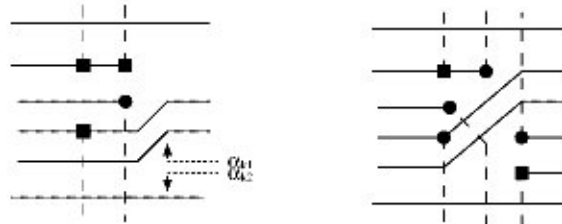

Fig. 11.   (a) Case 2.2.2 where $d + 1$ tracks are necessary; (b) improvements if layer reservation for diagonals is relaxed.

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          accordingly; /* as in the Case 1 of Theorem 1 */
          freetrack(c_i) := freetrack(c_{i-1}) - 1;
   (d)    if #new-net(c_i) = 2 then
              if freetrack(c_{i-2}) ≥ 1 then assign tracks for new nets
                 and set diagonals accordingly; /*as in Case 2.1 */
                 freetrack(c_i) := freetrack(c_{i-1}) - 2;
              else if freetrack(c_{i-2}) = 0
              /* two nets say, α_{j1} and α_{j2} (j1 < j2) must terminate in column c_{i-1};
                 let nets α_{k1} and α_{k2} (k1 < k2) begin in column c_i */
              if (j1 < k1 < j2) or (k1 < j1 < k2) then
                 assign tracks and diagonals as in Case 2.2.1;
                 freetrack(c_i) := freetrack(c_{i-1}) - 2;
              else insert an extra track;
                 Make height d + 1 and assign tracks and diagonals as in
                 Case 2.2.2; freetrack(c_i) := freetrack(c_{i-1}) - 1; /* h = d + 1 */
   (e)    Complete vertical connections and place vias appropriately.
          i := i + 1
   until i := l + 1;
end.
```

Example 1.   In the example shown in Figure 10, the via count is 32 and the total wirelength is 254.31, of which the length of diagonal wire segments is 11.31.

Remark.   The height of the channel increases from d to $d + 1$ only in the situation described in Case 2.2.2. However, if the diagonal wiring segments are allowed to occupy both the layers, then it may be possible to route in d tracks only (Figure 11).

Table I. Results on Benchmarks with Acyclic VCG in
Reserved Layer MD Model

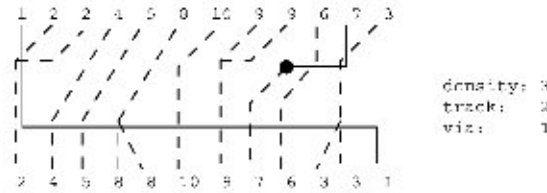| Example	Density (d)	v_{max}	Number of tracks (h)
YK$_{3a}$	15	4	15
YK$_{3b}$	17	9	17
YK$_{3c}$	18	6	18
DDE	19	23	19
Ex. 1 (Figure 10)	9	13	10

Fig. 12.   Routing of Burstein's difficult channel in the unreserved layer MD model.

Complexity.   Step 1 can be performed in $O(l)$ time. Step 3 iterates l times and requires $O(d)$ time in each iteration. Thus the overall complexity of the algorithm is $O(l.d)$, that is, linear in the area of the channel. The router needs at least d tracks, and at most $d + 1$ tracks. The space complexity is also $O(l.d)$.

4.3 Experimental Results

We have run our algorithm on standard routing benchmarks (YK$_i$ denotes the ith example of Yoshimura and Kuh [1982]) and the Deutsch difficult example (DDE) [Deutsch 1985], whose VCGs are acyclic. The algorithm terminates very fast and outputs routing with a channel height (h) equal to density (d) in each of these cases. A contrived example (Example 1) shown in Figure 10 requires $d + 1$ tracks. Results are given in Table I. It may be observed that the channel height h is independent of the length (v_{max}) of the longest directed path in VCG.

5. CHANNEL ROUTING IN UNRESERVED LAYER MD MODEL

If the VCG contains one or more directed cycles, no topological ordering of nets is possible. In other words, ordering of track assignment cannot remain invariant in all columns. In the reserved two-layer Manhattan model, a channel with a cyclic VCG may not be routable unless a suitable column (or a blank column) is found to accommodate a dogleg. In the unreserved layer or knock-knee model, this problem is relatively easy to tackle. In the unreserved layer MD model, cycles in VCG can be handled by using overlapping of nets in different layers, or by X- or swap routing [Chaudhary and Robinson 1991] as explained below in Section 5.1.

The height of a channel, number of vias and wire length can be significantly reduced using an unreserved layer MD router. Figure 12 shows the output of the proposed router for the Burstein's difficult example (BDE). Its VCG has directed cycles. An earlier solution [Ho et al. 1991] has three tracks and three vias, whereas our router uses two tracks and one via and smaller wire length.
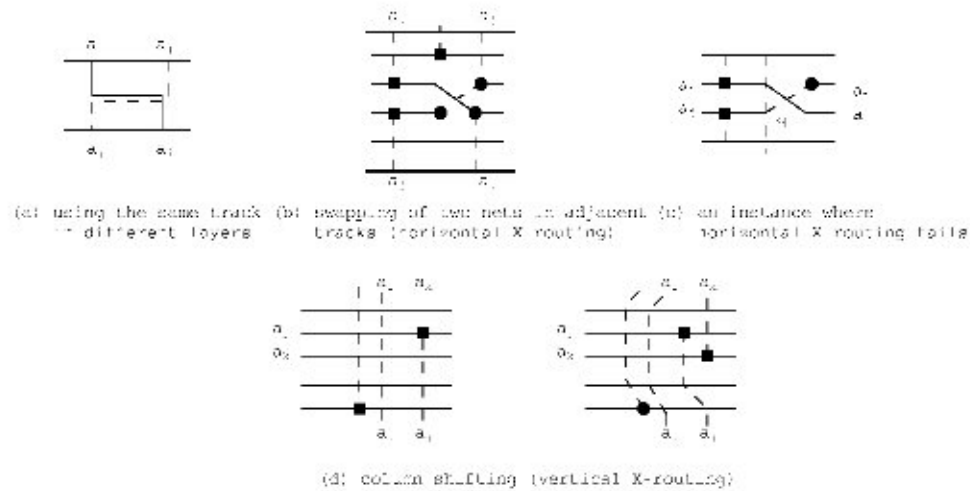
(a) using the same track (b) swapping of two nets in adjacent (c) an instance where
   in different layers   tracks (horizontal X routing)   horizontal X routing fails

(d) column shifting (vertical X-routing)

Fig. 13.   Resolving cyclic conflict in the unreserved layer MD model.

5.1 Resolving Cyclic Conflicts in VCG

(a) If the VCG has a cycle, there exist two nets that appear in some column c_i in reverse order. To continue routing one needs to swap the track assignments. If these two nets are routed in different layers (Figure 13(a)), the conflict can be avoided. If they are in the same layer in column c_{i-1}, we can use horizontal X-routing provided they occupy adjacent tracks (Figure 13(b)). However, there are cases (Figure 13(c)) where this cannot be done because of nonavailability of via space at the grid point g. Cyclic conflict can also be eliminated by using vertical X-routing and column shifting (Figure 13(d)).

(b) The number cyclic conflicts can be considerably reduced if we pick up minimum number of edges whose removal renders the remaining VCG acyclic. This calls for solving the minimum feedback arc set (MFAS) problem in a directed graph, which is known to be NP-complete for general graphs [Garey and Johnson 1979]. We use a linear-time greedy heuristic based on depth-first search for solving MFAS.

5.2 Theme of the Algorithm

We now present a greedy algorithm for routing a channel in the unreserved layer MD model. First, the VCG is made acyclic by removing a minimal set of edges. This identifies the columns where nets are to be swapped. The resultant VCG is sorted topologically to determine a linear ordering of nets. We assume $\lceil d/2 \rceil$ tracks are available initially.

The algorithm routes the nets in column-by-column fashion as before. Since horizontal segments in two layers may overlap, effectively we have d tracks to start with. Tracks are assigned to nets following the order, and diagonals are inserted if necessary when new nets appear. Cyclic conflicts are resolved using overlaps or X-routing. New tracks are inserted whenever necessary. Vertical connections are implemented using straight wire segments and minimum vias,
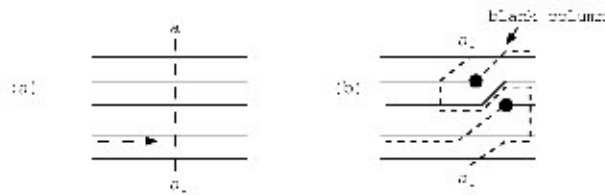
Fig. 14. Vertical connection in the unreserved layer model using a blank portion of the next column.

and if no such path is found, the possibility of rerouting it through its neighborhood is examined (Figure 14), or a maze router [Sherwani 1999] is called on the grid structure of Figure 3. If the maze router fails, an extra track (or a blank column) is inserted to complete the vertical connection. The algorithm is formally described below.

5.3 Algorithm 2: MD-CU (Unreserved Layer MD Channel Router)

Input: A channel C of length l, a netlist of n nets, and two routing layers.
/* Let $c_1, c_2, \ldots, c_l$ denote the columns ordered from left to right */.
Output: Unreserved layer MD routing.

begin
Step 1. (a)   Construct the VCG and make it acyclic
                   by removing minimum number of edges in a simple greedy way;
        (b)   Topologically sort the nodes of the acyclic VCG;
                   construct a linearly ordered sequence of nets $\{a_1, a_2, \ldots, a_n\}$;
        (c)   Determine the density d of C;
        (d)   freetrack-layer-1(c_0) = $\lceil d/2 \rceil$; freetrack-layer-2(c_0) = $\lceil d/2 \rceil$;
                   /* initially, d tracks are free in C */
        (e)   i := 1;
Step 2. Repeat
        (a)   if leftmost or rightmost terminal of any net does not appear in column c_i
                   then track assignment in column c_i is same as in column c_{i-1};
        (b)   if r nets (r = 1 or 2) terminate in column c_i then mark the free tracks and
                   increment the freetrack count of the two layers accordingly;
        (c)   if #new-net(c_i) = 1 then
                   if freetrack-layer-1(c_{i-1}) > 0 then q := 1, TRACK(q);
                   else if freetrack-layer-2(c_{i-1}) > 0 then q := 2, TRACK(q);
                       else insert a free track in a position satisfying the topological order,
                           and assign the net in layer 1;
                           freetrack-layer-2(c_i) := freetrack-layer-2(c_{i-1}) + 1;
        (d)   if #new-net(c_i) = 2 then
                   if freetrack-layer-1(c_{i-1}) > 1, then call step 3(d) of Algorithm 1
                   else if freetrack-layer-1(c_{i-1}) = 1 then
                       if freetrack-layer-2(c_{i-1}) > 0 then
                       q := 1, TRACK(q), q := 2, TRACK(q)
                       else insert a free track in a position satisfying the topological order
                           and call step 3(d) of Algorithm 1;
                           freetrack-layer-2(c_i) := freetrack-layer-2(c_{i-1}) + 1;
                   else insert a free track in a position satisfying the topological order;
                       q := 1; TRACK(q), q := 2; TRACK(q);
        (e) /*let $a_i(a_j)$ be the net to be connected to top (bottom) terminal in column c_i.*/
               if tracks t_i, t_j assigned to a_i, a_j (resp.) are in the same layer
                   and occupy adjacent tracks in column c_{i-1},

and the edge (a_i, a_j) was removed from the VCG in Step 1(a)
then interchange tracks assigned to a_i, a_j by X-routing;
else skip this step;
(f) Vertical-Connect $((g(t_i, c_i)), (top(c_i)))$;
Vertical-Connect $((g(t_j, c_i)), (bottom(c_i)))$;
Place vias appropriately.
$i := i + 1$;
until $i := l + 1$;
end.

Procedure TRACK(q)

begin
locate track t_i in layer q that satisfies topological order including incoming nets;
make the track free by using diagonal connections from grid points in column c_{i-1}
and assign the tracks in column c_i accordingly;
freetrack-layer-$q(c_i)$:= freetrack-layer-$q(c_{i-1}) - 1$;
end;

Procedure Vertical-Connect $((g(t, c_i))$, (top/bottom$(c_i)))$

/* g is a grid point formed by intersection of a horizontal track t and column c_i, and top/bottom(c_i) denotes the top or bottom terminal in column c_i. The goal is to interconnect these two points. */

begin
1. if vertical connection possible then
connect them by a vertical wire using one or both layers and vias;
else if re-routing is possible, as in Figure 13 or Figure 14 then re-route;
else call maze router in sub-grid bounded by c_k and c_i;
/* c_k denotes the column where the maze router was called last; initially,
$k = 1$. */
2. if maze router fails then add a new horizontal track in the required position
or a blank column (between c_i and c_{i+1});
re-adjust tracks using diagonals; complete the interconnection using a vertical
wire;
end;

Complexity.   The VCG is made acyclic by removing minimal number of edges using a greedy heuristic based on depth-first search. Thus, Step 1 can be performed in $O(l)$ time. Step 2 iterates l times and Steps 2(a)–(d) require $O(l.h)$ time over l iterations as before, where h is the channel height. Step 2(e) takes $O(l)$ time. Completion of vertical connections as well as placement of vias in Step 2(f) takes $O(l.h)$ time over l iterations, because the search space in the $(l \times h)$ grid on which the maze router is called is distinct in each call. Thus, the overall complexity of the algorithm is $O(l.h)$, that is, linear in area of the channel. The space complexity is also $O(l.h)$. The time complexity of the router shows significant improvement over those reported earlier [Chaudhary and Robinson 1991; Ho et al. 1991; Pal et al. 1995; Yoshimura and Kuh 1982].

5.4 Experimental Results

We have implemented the algorithm using a heuristic for the MFAS problem and a simple maze router. Table II compares its performance with the results obtained in the Manhattan model [Deutsch 1985; Ho and Iyengar 1989; Ho et al. 1991; Reed et al. 1985; Rivest and Fiduccia 1982; Yoshimura and Kuh

Table II. Number of Tracks for Benchmark Examples

Example	Density	Number of tracks by earlier routers (two layers)	Proposed router in MD-model		
			#tracks	#extra blank columns	#calls to maze router
YK_{3a}	15	15[a]	13	0	3
YK_{3b}	17	17[a]	15	0	2
$YK_{3c,1}$	18	18[a]	17	0	1
$YK_{3c,2}$			16	1	1
DDE*	19	19[b,c,d]	18	0	0
CR	19	17[e]	17	0	0
BDE† (Figure 12)	4	3[c]	2	0	0
Cyde.tough	16	16[f]	15	0	0
			14	1	3

*—Deutsch's difficult example; †—Burstein's difficult example; entries within square brackets indicate references.
[a] Yoshimura and Kuh [1982].
[b] Burstein and Pelavin [1983].
[c] Ho et al. [1991].
[d] Reed et al. [1985].
[e] Chaudhary and Robinson [1991].
[f] Ho [1989].

Table III. Comparison of the Number of Vias and Wire Length

Example	Number of vias			Wire-length		
	Router output	Via minimizer[a]	Proposed method	Router output	Algorithm[a]	Proposed method
YK_{3a}	91[b]	66	57	1365	1362	1228.37
YK_{3b}	107[b]	78	66	1651	1653	1540.40
YK_{3c}	125[b]	103	99	2100	2100	2061.30
YK_{3c}	125[b]	103	97	2100	2100	2027.54
DDE	301[c]	226	225	4989	5058	4909.64
BDE	3[d]	—	1	71	—	56.04

[a] The et al. [1991].
[b] Yoshimura and Kuh [1982].
[c] Deutsch [1985].
[d] Ho and Iyengar [1989].

1982] and the diagonal model [Chaudhary and Robinson 1991]. The benchmark YK_{3c} has been considered as two separate cases $YK_{3c,1}$ and $YK_{3c,2}$ depending on the number of tracks used. The example CR is taken from [Chaudhary and Robinson 1991]. Experimental evidence reveals that our solutions compare favorably with the best-known existing results with respect to channel height and, consequently, channel area. Using two layers, the proposed method outputs 18 tracks for DDE, and two for BDE (Figure 12). The algorithms are simple, easy-to-implement, and produce outputs in linear time. As seen from Table II, only a few calls are made to the maze router. The number of vias and total wire length also improve compared to those in The et al. [1991] and Yoshimura and Kuh [1982] (Table III). It may be noted that smaller via counts for the benchmark examples YK and Deutsch are obtained by using the topological channel router [Haruyama et al. 1992]. Similar via reduction techniques may be adopted in our algorithm for further improvement.
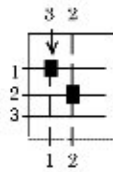
Fig. 15.   Three-sided channel.

6.   ROUTING L-CHANNELS

Among the previous attempts, the Manhattan router by Chen [1987] divides an L-channel into a vertical channel with terminals on opposite sides, routed by one of the standard Manhattan channel routers, and a horizontal channel with terminals on three sides—its routability cannot be ensured always in the Manhattan unreserved layer model without increasing channel height. For the example in Figure 15, it is not possible to connect the top terminal for net 3 with that on the left vertical side using two layers. This is owing to the fact that the vertical constraints on the left side conflict with that for column 1.

   With 45° wires, Chen's [1987] method maps an L-channel entirely into a straight channel, routes it by the standard reserved layer Manhattan router, and then replaces all the vertical wires by diagonal wires. However, there are two triangular regions at both ends of the L-shaped region, which have to be routed later on; this was not taken care of explicitly [Chen 1987]. If the two subchannels are of the same density, this easy method gives a space-efficient solution. Since the channel boundary can be moved in the 45° direction only, the less dense subchannel may have empty tracks unless a refinement pass is carried out. The second major disadvantage of Chen's [1987] approach is that it uses many long diagonal wires that may not only increase the wire length but also the probability of manufacturing defects even under the modified set of design rules shown in Figure 2. In another approach [Maddila et al. 1989], an L-channel is divided into three parts, namely two straight channels and a special switchbox junction with fixed terminals on two adjacent sides. The junction is routed first and then the two three-sided straight channels assuming the knock-knee model. An efficient routing algorithm in the MD model to overcome the above-mentioned shortcomings is presented in this section. This algorithm relies on solving the triangular routing problem described next.

6.1 Scheme for L-Channel Routing

In the proposed method, the L-channel is first split into two subregions A and B (Figure 16a), each of which is further decomposed into a two-sided channel and a triangular region (Figure 16(b)). In this scheme, the triangular region is located near the L-junction, as opposed to that at the open end of the L-channel in Chen's [1987] algorithm. The vertical subchannel A is virtually rotated by 90° and placed to the left of the subchannel B, as illustrated in Figure 16(c), to form a straight channel C. The density of this channel is computed and the terminals are routed by a standard Manhattan channel router [Yoshimura and Kuh 1982]. It should be ascertained that no doglegs are inserted by the router
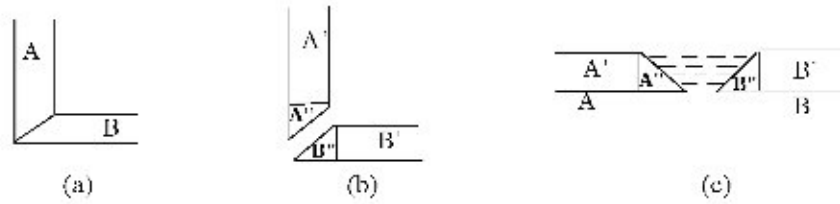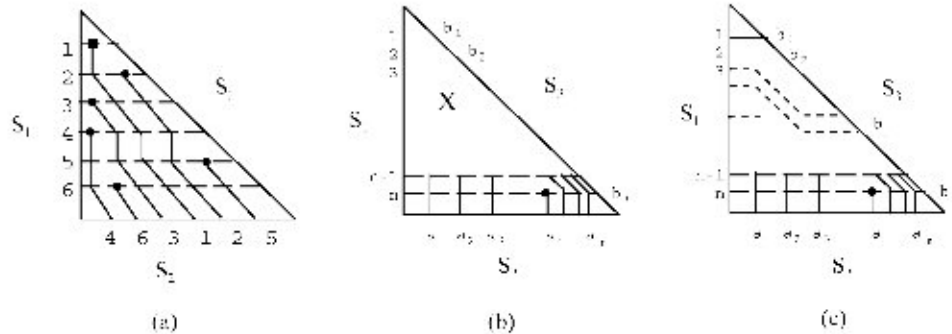
Fig. 16.   Key steps of MD-L.

Fig. 17.   Triangular routing.

in the triangular regions A'' and B''. Thus, track assignment for the nets is accomplished in the regions A' and B' and the sequence of nets is identical along the two hypotenuses of triangular regions A'' and B''. Finally, algorithm MD-T, described below, completes the triangular routing within A'' and B''. If extra columns are required by MD-T for A'' (B''), then the subregion A' (B') is slightly rerouted accordingly by using a few diagonal wire segments. The novelty of this algorithm lies in the routing of the L-junction in the MD model; most of the channel has Manhattan wiring, hence achieving smaller wire-length. The time complexity remains proportional to the area of the L-shaped routing region.

6.2 Triangular Channel Routing

Consider an isosceles right-angled triangular routing region where S_1 and S_2 are its two equal sides, and S_3 its hypotenuse (Figure 17(a)). Without loss of generality, let the terminals on S_1 be distinct and labeled $< 1, 2, \ldots, n >$. Any terminal on the other two sides has a label i, $0 \leq i \leq n$, where 0 represents a null terminal. The objective is to connect all the nets within the triangular area; reducing via count and/or wire length may be a secondary goal. Several cases may arise.

Case 1:   The sequence of terminals on S_3 is same as that of S_1, and the sequence of terminals on S_2 is a permutation of $< 1, 2, \ldots, n >$.

LEMMA 1.   An instance of Case 1 is always routable in the MD model within the triangular area.

PROOF. For $n = 2$, routing in the triangular area is trivial. Suppose the lemma holds for $n - 1$ nets. For the induction step, consider the triangular routing problem for n nets with the sequence of terminals on S_1 and S_3 as $< 1, 2, \ldots, n >$, and that on S_2 as $< a_1, a_2, \ldots, a_n >$, which is a permutation of $< 1, 2, \ldots, n >$. Thus, the respective terminals on S_1 and S_3 can be connected using horizontal tracks. Let $a_i = n$; then it can be connected to the nth horizontal track using a vertical segment. Vertical wire segments from all terminals to the left of a_i and diagonal segments from all terminals to the right of a_i up to the $(n - 1)$th horizontal track are inserted (not necessarily connected). This yields a triangular region X (Figure 17(b)) having $n - 1$ nets, which by the induction hypothesis, is routable within the region X itself. Hence the lemma is proven. □

Case 2: Some of the nets may have more than one terminal on S_2, while some terminals may be 0. Each net appears at least once either on S_1 or S_3. There are two subcases.

Case 2.1: The terminals on S_1 and S_3 appear as identical sequences.

LEMMA 2. An instance of Case 2.1 is routable in the MD model within the triangular area if, for every i on S_1, the number of terminals on S_2 having labels in the set $\{0, i + 1, \ldots, n\}$ is at least $(n - i)$.

PROOF. The respective terminals on S_1 and S_3 can be connected by horizontal tracks as their sequences are identical. For any net j, its terminals on S_2, if any, have to be connected to the jth horizontal track using vertical and diagonal wire segments. By reasoning as in Lemma 1, for any net i, the triangular region above the ith horizontal track is routable if the number of nets (whose terminals are on S_2) that are yet to be routed is less than i. □

Case 2.2: The terminal sequences on S_1 and S_3 are different.
Let the number of nets in the triangular region consisting of those on S_1 and S_3, be $n + k$. Any terminal on S_2 belongs to a net that also has a terminal on either S_1 or S_3 or both. Let $< b_1, b_2, \ldots, b_n >$ be the sequence of terminals on S_3, and, for any i, the label b_i belongs to $\{1, 2, \ldots, n + k\}$. Now we study the following subcases.

Case 2.2.1: If terminals of any net appear on both S_1 and S_3, then their corresponding indices in S_1 and S_3 are equal, that is, $i = b_i$. This is the case of nondogleg.

LEMMA 3. An instance of Case 2.2.1 is routable in the MD model within the triangular area if both the following conditions hold: (i) for any i, $i \neq b_i$, all the terminals of net i on S_2 are to the left of those of net b_i on S_2, and (ii) for any i on S_1, the number of terminals of S_2 belonging to the nets in $\{1, 2, \ldots, i - 1\} \cup \{b_1, b_2, \ldots b_{i-1}\}$ is less than i.

PROOF. The terminals of nets which appear on both S_1 and S_3 are connected by horizontal tracks, as $i = b_i$. For $i \neq b_i$, terminals belong to different nets so the corresponding horizontal track is shared by the two

nets with the left segment occupied by net $i \in S_1$ and the right segment of the track by net $b_i \in S_3$. For any net j, its terminals on S_2, if any, are connected to the jth horizontal track using a sequence of vertical and diagonal wire segments. This can be achieved only if all terminals of net i appear to the left of all terminals of net b_i on S_2. In fact, the terminals on S_2 for all the nets that have one end point on S_1 and the other end on S_2 alone must be to the left of the terminals of all the nets in the set $\{n+1, n+2, \ldots, n+k\}$ appearing on both S_2 and S_3.

Now, as in Lemma 1, the triangular region above the ith horizontal track for any i is routable if the number of terminals on S_2 yet to be routed is less than i. These terminals must belong to the nets in $\{1, 2, \ldots, i-1\} \cup \{b_1, b_2, \ldots b_{i-1}\}$. □

Case 2.2.2: If terminals of any net appear on both S_1 and S_3, then their corresponding indices in S_1 and S_3 may not necessarily be equal, that is, on S_1 there may exist an i such that $b_i \in S_3$ is a terminal of net $j \neq i$.

This is a case of doglegging (Figure 17(c)), and may require extra horizontal track and/or column if $i = b_j$ where $j \neq i$. However, in the context of L-channel routing, algorithm MD-L (described later) never spawns off an instance of this case. This no-dogleg criterion is required as mentioned in Section 6.1 above.

We now present the algorithm MD-T for routing a triangular channel. Let the total number of nets appearing on the sides S_1 and S_3 be $n+k$, for some $k \geq 0$. The nets are assigned index numbers from 1 to $n+k$ according to the sequence of n terminals on side S_1 first, and then the sequence of terminals on S_3 of the remaining k nets not appearing on S_1. Henceforth, in the algorithm MD-T presented below, the terminals will be referred to by the index numbers corresponding to their nets.

6.3 Algorithm 3: MD-T (for Triangular Routing)

Input: Terminal lists $< a_1, a_2, \ldots, a_n >$ and $< b_1, b_2, \ldots, b_n >$ on S_2 and S_3, respectively.
Output: MD-routing within the triangular area T.

```
begin
    l := 0; /* l is leftmost column used and is initially the left boundary of T */
    c := l; /* c denotes the rightmost column with null terminal on S₂ and
            is initialized to the leftmost column along the left boundary of the triangle */
    for i := n downto 1 do
        begin
            if null terminal exists in row i then c ← rightmost null terminal
                else l := l − 1 ; c := l;
            insert diagonal wire segments in layer 1 between rows i and i − 1
                for nets of S₂ from right to left up to column c;
            forall terminals or endpoints of wire segments to the left of column c do
                insert vertical wire segments in layer 1 between rows i and i − 1;
            if i = bᵢ then
                begin
                    insert horizontal wire segments connecting i and bᵢ in layer 2;
                    insert via(s) from diagonal/vertical wire segment(s) of net i in layer 1
                        to horizontal wire segments of the same net in layer 2;
```

```
/* S₂ is updated such that nets connected to vias in row i are replaced by 0
            and then the cᵗʰ element is deleted */
        forall aⱼ ∈ S₂ do if aⱼ = i then aⱼ = 0;
        S₂ :=< a₁, a₂, ..., a_{c−1}, a_{c+1}, ..., aₙ >;
    end;
  if bᵢ ∉ S₁ then
      begin
        if on S₂, rightmost terminal of net i is left of leftmost terminal of net bᵢ
        then net i and bᵢ share the same track
        else insert a horizontal track between rows i and i − 1;
        insert horizontal wire segments for i and bᵢ in layer 2;
        insert via(s) to connect diagonal/vertical wire segments of net i and bᵢ
            in layer 1 to horizontal wire segments of the same net in layer 2;
        forall aⱼ ∈ S₂ do if aⱼ = i or aⱼ = bᵢ then aⱼ = 0;
        S₂ :=< a₁, a₂, ..., a_{c−1}, a_{c+1}, ..., aₙ >;
        /* update S₂ by removing cᵗʰ entry */
      end;
  endfor;
end.
```

THEOREM 2.   Algorithm MD-T produces a valid routing.

PROOF.   It has been pointed out earlier that as algorithm MD-L is designed to be dogleg-free, it can generate only the Cases 1, 2.1, or 2.2.1 of MD-T, as mentioned above. The routability criterion for each of these cases is given, respectively, by Lemmata 1, 2, and 3 above. If the criterion of the lemma corresponding to the case is not satisfied, then an extra track or column, as the case may be, is added. Hence, the theorem follows. □ .

Time complexity: The time complexity of algorithm MD-T is $O(n^2)$, that is, linear in the area of the routing region. Horizontal and vertical wires are on the reserved layers and thus cannot overlap, but diagonal wires may appear in either layer and can overlap.

6.4 L-Channel Router MD-L

In detailed channel routing, it has been observed that the channel height is strongly influenced by the alignment of terminals on the two sides of the channel [Ohtsuki 1986], that is, if the terminals on one of the two sides are shifted with respect to those on the other, the alignment of terminals may change and hence the channel density. It incurs an inherent tradeoff between routing area and wirelength. Thus, a significant feature of our L-channel routing algorithm MD-L, based on the scheme discussed in Section 6.1, is the step of virtual terminal alignment for further reduction in channel density.

The terminal alignment that minimizes the density of an L-channel is obtained as follows. Suppose the vertical subchannel A of an L-channel, after virtual rotation by 90°, has top and bottom boundaries ab and pq, respectively (Figure 18). If point b is aligned with point q by right-shifting the terminals on ab with respect to pq, then the density may change. Let $d_A(0)$ and $d_B(0)$ be the original densities of the given subchannels A and B. Suppose nets $< n_1, n_2, \ldots, n_k >$ occur in both A and B. The operation $move_A(m)$ is defined as
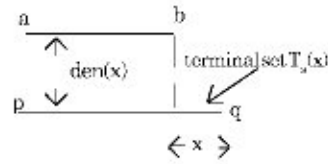
Fig. 18.   Pin alignment in MD-L.

a right shift of the terminals on ab by m columns. The corresponding density of A is denoted by $d_A(m)$, and the set of m rightmost terminals on pq, the lower boundary of A, by $T_A(m)$ (Figure 18). It may be noted that the right shift cannot be greater than the original height of the channel. As the actual height is unknown before routing, the best way to approximate the height is by calculating channel density $d(m)$. Similar definitions hold for the horizontal subchannel B of the L-channel, except that for the operation $move_B(r)$, terminals on the bottom boundary of B are left-shifted by r columns. Suppose the densities of subchannels A and B are minimum for their respective move operations by m and r columns. The minimum possible density of the entire L-channel under this terminal alignment scheme is then given by

$$d_{min} = \min_{m<d_A(0),r<d_B(0)} (\max(d_A(m), d_B(r), m, r, |P|)), \qquad (1)$$

where $P = T_A(m) \cup T_B(r) \cup \{n_1, n_2, \ldots, n_k\}$.

6.5 Algorithm 4: MD-L (for L-Channel Routing)

Input: Sequence of terminals along the border of an L-channel.
Output: MD-routing within the L-shaped area.

begin
Step 1.   Initially rotate sub-channel A by 90° and place it to the left of sub-channel B;
Step 2.   Determine d_{min} for L-channel and corresponding values of m and r using
                eqn. (1);
              Shift the terminals on the bottom boundaries of A and B by m columns right
                  and r columns left respectively to obtain a straight channel C;
Step 3.   Route the straight channel C by a greedy router [Ho et al. 1991];
                /*Let h be the height of the channel.*/
Step 4.   Form triangular region for A with topmost m tracks and rightmost m
                  columns;
              Route the triangular region by the procedure MD-T;
              Form triangular region for B with topmost r tracks and leftmost r columns
                  and route the triangular region by MD-T;
              Move terminals on the bottom boundaries of A and B by shifting
                  $x = h - m$ columns right, and $x' = h - r$ columns left respectively;
              Shift m and r bottommost tracks in A and B accordingly
                  and replace vertical wire segments by appropriate diagonal segments;
Step 5. Place routing output from Step 4 in the form of L-channel
                  by joining the corresponding ends of A and B;
              Scan A from bottom to top and B left to right for removal of diagonal
                  segments in unreserved layer model wherever room is available
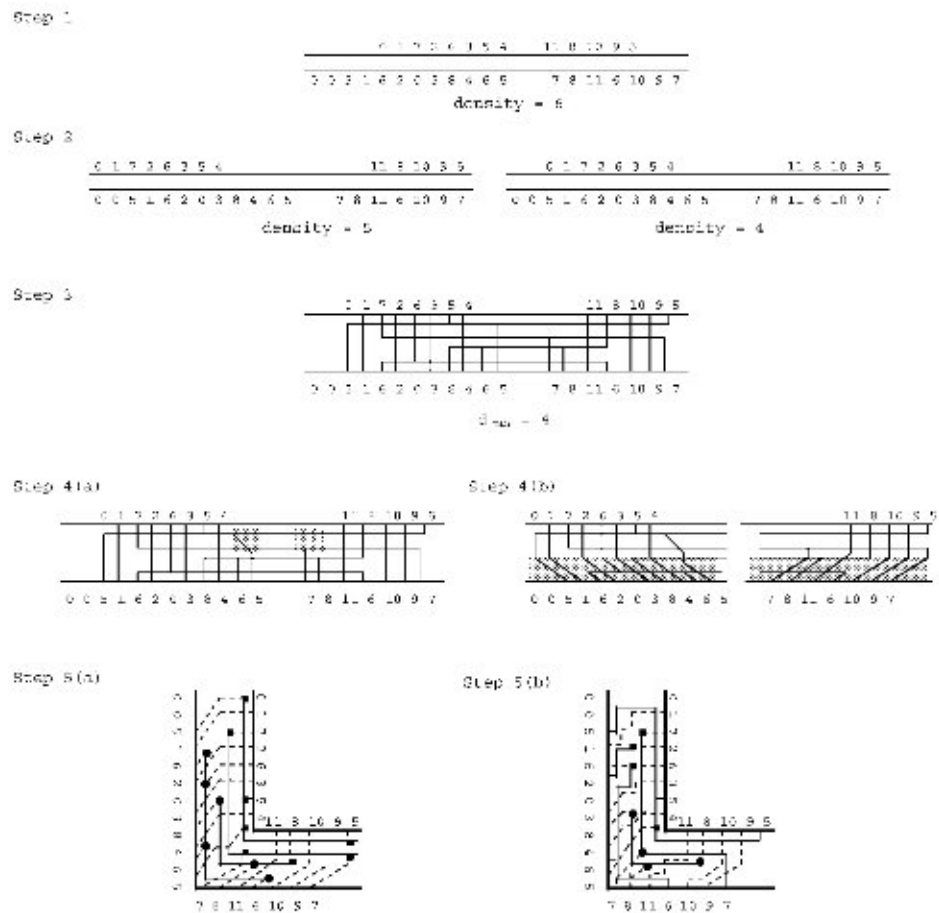   (Figure 19);
end.

Fig. 19. Routing steps in MD-L for Example 2.

In Step 3, this algorithm scans the terminals in the channel C from left to right. A greedy router [Ho et al. 1991; Sherwani 1999] is then used to complete the routing for one column before proceeding to the next. A greedy router can handle cyclic constraints in the VCG that may arise during shifting of terminals. If no cyclic constraints are introduced after virtual terminal alignment corresponding to d_{min}, an MD router for reserved layer can be used as it guarantees a solution with at most $d_{min} + 1$ tracks.

The steps of the proposed L-channel router (MD-L) have been illustrated with an example (Example 2) in Figure 19.

Time complexity: The time complexity of MD-L is $O(l \cdot d_{min})$ where l is the length of the straightened L-channel and d_{min} is the minimum channel density obtained by terminal alignment.

6.6 Experimental Results

The total length of diagonal wires, height of the L-channel, and the number of vias in the routing solutions produced by algorithm MD-L for five difficult
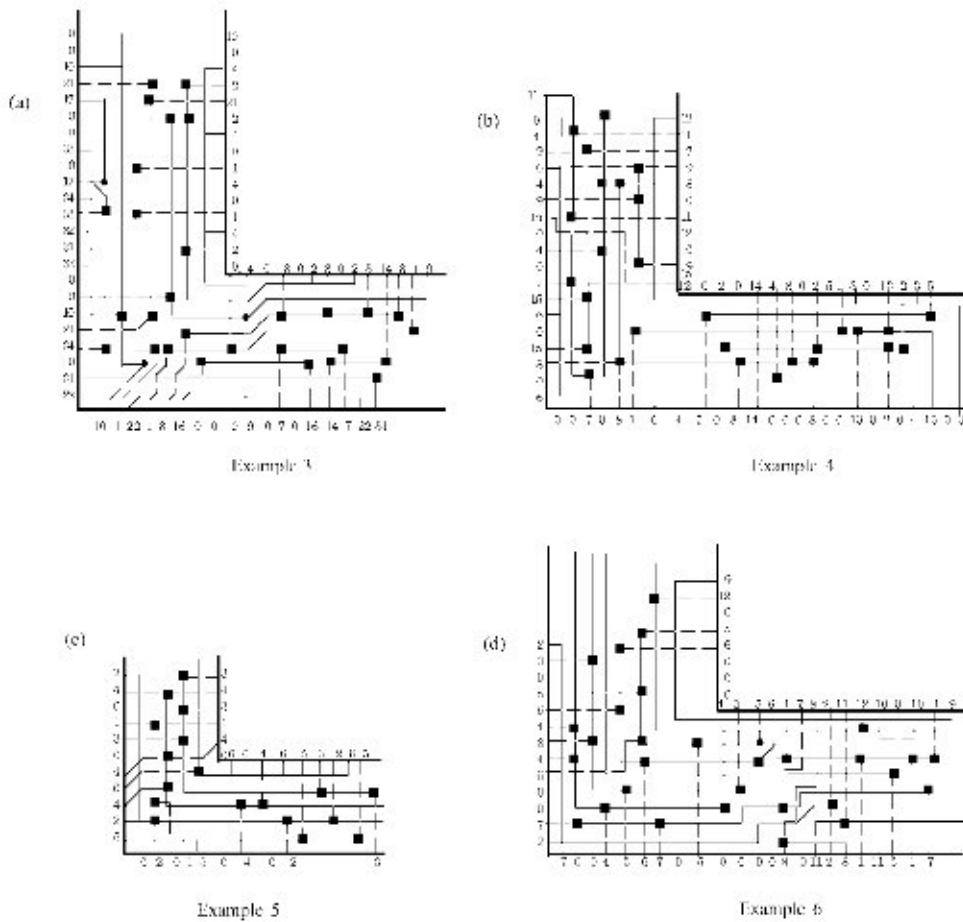
Fig. 20.   Routing produced by MD-L for four problem instances.

examples (Figures 19–21) are summarized in Table IV. Comparison of this algorithm's performance with that of Chen's [1987] algorithm is also made. In the routing solutions shown in Figures 19–21, the via count is found to be significantly smaller; the circular vias, in the figures depict the recommended octagonal vias, and these account for less than 10% of the total via count.

Algorithm MD-L is easy to implement and terminates very quickly. In addition to routing several L-channels, an instance of a nonslicible floorplan (Example 7, Figure 21) has been constructed, which has one L-channel and three straight channels. Of these three, one is an instance of Burstein's difficult channel [Joobani 1986] and another of YK1 [Yoshimura and Kuh 1982]. The L-channel has been routed with the proposed MD-L, Burstein's channel with the MD unreserved layer channel router, and the remaining two straight channels including YK1 by a standard Manhattan router [Yoshimura and Kuh 1982]. This demonstrates an efficient routing with minimum area for an entire floorplan.
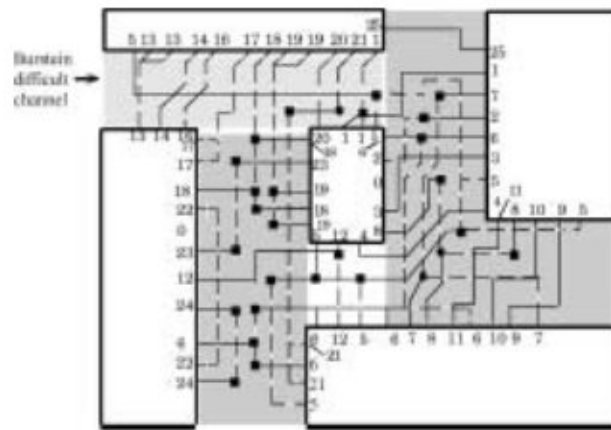
Fig. 21.   Example 7 routed by MD-L.

Table IV.   Performance of the Proposed MD-L Router

Example	Diagonal wirelength		# tracks		# vias	
	Chen [1987]	MD-L	Chen [1987]	MD-L	Chen [1987]	MD-L
Ex. 2 (Figure 19)	*	$9\sqrt{2}$	*	4	*	7
Ex. 3 (Figure 20(a))	*	$19\sqrt{2}$	*	8	*	32
Ex. 4 (Figure 20(b))	$220\sqrt{2}$	0	10	7	62	29
Ex. 5 (Figure 20(c))	$11\sqrt{2}$	$4\sqrt{2}$	8	5	36	18
Ex. 6 (Figure 20(d))	$130\sqrt{2}$	$2\sqrt{2}$	11	9	51	31
Ex. 7 (Figure 21)	*	$23\sqrt{2}$	*	†	*	28

*—not available; †—not applicable.

7. ROUTING IN SWITCHBOXES AND STAIRCASES

A placement may have cross-junctions (Figure 23(a)) where four channels meet. The routing in this junction region can be carried out by redefining the cross-junction as one L-channel and two straight channels. However, there may still be the need for handling switchboxes (Figure 22(a)) by themselves.

7.1 Switchbox Routing

Given an instance S of switchbox routing with k rows and m columns, let $< l_1, l_2, \ldots, l_k >$ and $< r_1, r_2, \ldots, r_k >$ be the sequence of nets from top to bottom on the left and right sides, respectively, and $< t_1, t_2, \ldots, t_m >$ and $< b_1, b_2, \ldots, b_m >$ be the sequence of nets from left to right on the top and bottom sides, respectively. We define a switchbox constraint graph, SCG as a supergraph of the VCG, as illustrated in Figure 22. The VCG is first formed using the terminals on the top and bottom sides (Figure 22(b)), and then for each of the two sequences on the left and right sides, the VCG, which is a chain of directed arcs (Figures 22(c) and (d)), is added to obtain the SCG (Figure 22(e)). The SCG corresponds to an instance of an equivalent two-sided channel C (Figure 22(f)).
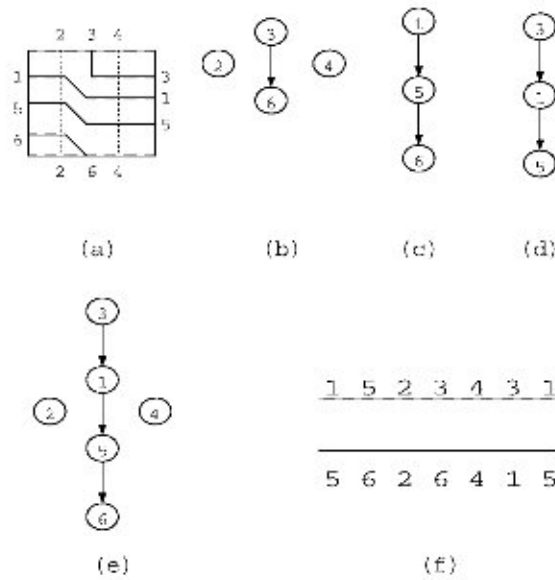
Fig. 22. (a) An instance of switchbox routing, (b) VCG for the top and the bottom rows, (c) VCG for the left side, (d) VCG for the right side, (e) resultant Switchbox Constraint Graph (SCG), (f) equivalent two-sided channel.
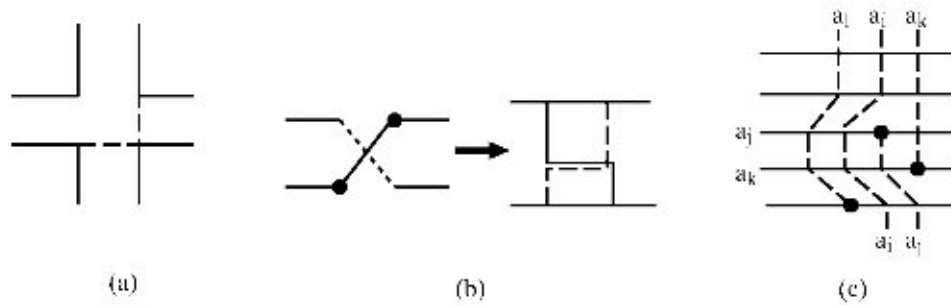

Fig. 23. (a) Cross junction; (b) swap routing, (c) rerouting.

For a given switchbox S, we construct a straight channel C_S as follows :

$TOP = <l_1, l_2, \ldots, l_{k-1}, t_1, t_2, \ldots, t_m, r_1, r_2, \ldots, r_{k-1}>;$
$BOT = <l_2, l_3, \ldots, l_k, b_1, b_2, \ldots, b_m, r_2, r_3, \ldots, r_k>.$

A routing solution of C_S is called satisfactory if $k - 1$ columns from the left and $k - 1$ from the right are dogleg free.

THEOREM 3.   (i) If a switchbox S has a solution with h rows, then the channel C_S has a satisfactory solution of height h.

(ii) If C_S has a satisfactory solution with h tracks, then the switchbox S has a solution with $\max(h, k)$ rows.

PROOF.   Follows from the construction of C_S.   □

If the SCG is acyclic, an ordered sequence of nets for assigning tracks is determined based on its equivalent channel C_S. For cyclic SCG, two nets or terminals with conflicting order can be handled by swap (Figure 23(b)) or X-routing [Chaudhary and Robinson 1991]. We now present the algorithms MD-SR and MD-SU for routing a switchbox using the reserved and unreserved layer MD model, respectively.

7.2 Algorithm 5: MD-SR (for Acyclic SCG)

Input: A switchbox S of size $(k \times m)$, a netlist of n nets, and two routing layers.
Output: Reserved layer MD routing (horizontal and $\pm 45°$ wires in one layer and vertical with $\pm 45°$ wires in other layer).

begin
    Step 1.   Construct the equivalent straight channel C_S;
    Step 2.   Route C_S by reserved layer MD channel routing algorithm;
    Step 3.   Extract the portion of the channel bounded within column i
             and column $(i + m - 1)$ for routing of S;
end;

Remark.   If the height h of C_S is greater than k, then the algorithm MD-SR needs $(h - k)$ extra tracks for routing the switchbox S. This may be improved by using a channel router in the unreserved layer MD model, as described next.

7.3 Algorithm 6: MD-SU (for General SCG)

Input: A switchbox S of size $(k \times m)$, a netlist of n nets, and two routing layers.
Output: Unreserved layer MD routing.

begin
    Step 1   Construct SCG and remove minimum number of edges to make it acyclic
             (minimum feedback arc set problem) by a simple greedy heuristic;
             Topologically sort the nodes of the acyclic SCG obtained;
             Construct a linearly ordered sequence of nets $\sigma = <a_1, a_2, \ldots, a_n>$;
    Step 2.   From left to right of S, assign nets in σ to horizontal tracks in layer 1;
             update the count of unused horizontal tracks;
             $i := 1$;
    Step 3.   Repeat
             (a) if two nets are in conflicting order at column c_i then re-adjust net
                assignment on tracks by swapping them in adjacent tracks
                (Figure 23(b)) [Chaudhary and Robinson 1991];
             (b) if a net terminates in column c_i
                then mark the respective horizontal track free,
                and update the count of unused tracks accordingly;
             (c) if new nets appear at column c_i then free the track according to σ,
                by shifting nets onto adjacent tracks by $45°$ routing as in Algorithm 2;
                insert an extra track if needed;
             (d)(i) Route top and bottom terminals in vertical columns on layer 2;
                  failing which both layers and vias are used
                    else check whether re-routing is possible (Figure 23c);
               (ii) else call maze router within sub-grid bounded by c_u and c_l
               (use horizontal, vertical and diagonal wires on both layers);
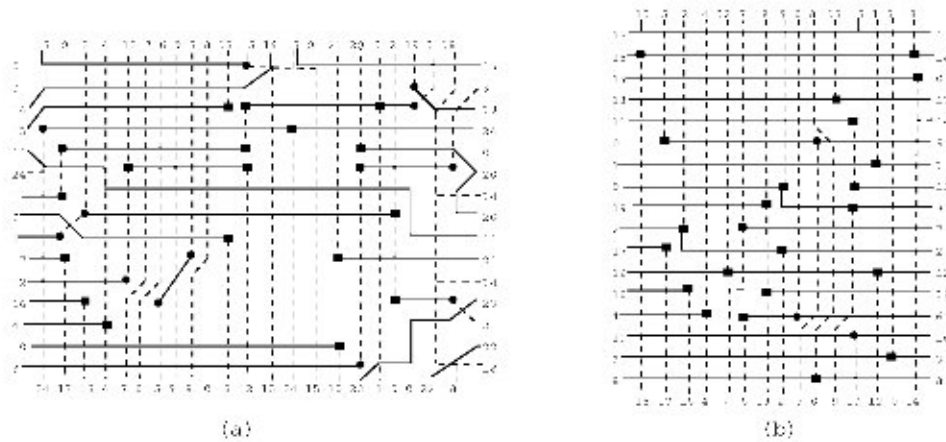
Fig. 24.   Routing of (a) Burstein's difficult switchbox (MD-SU), (b) dense switchbox (MD-SR).

Table V.   Performance of the Manhattan-Diagonal Switchbox Router

Switchbox example	# rows	# columns	(#extra rows, #extra columns)		
			In[a]	In[b]	proposed method
Burstein's (Figure 24(a))	15	22	(1,0)	(0,0)	(0,0)
Dense (Figure 24(b))	17	15	(0,1)	(0,1)	(0,0)

[a] Joobani [1986].
[b] Shin and Sangiovanni-Vincentelli [1986]; Tzeng and Sequin [1988].

/* c_u is the column where maze router was called last; initially $u = 1$. */
    (iii) if maze router fails then add an extra track or column accordingly;
(e) $i := i + 1$;
until $i := m$;

Step 4.   if more than one terminal of a net appear on left (right) boundary of S,
    then use diagonal moves to re-route
        and push the existing vertical segments towards right (left)
        till leftmost (rightmost) column is available;
    if the above fails then insert an extra column
        at the leftmost (rightmost) position;

end;

Time Complexity: The time complexity of routing a switchbox with k rows and m columns is $O(k \cdot m)$. Although a maze router may be called, each call is made on a distinct and disjoint subgrid.

7.4 Experimental Results

The proposed algorithm routes Burstein's difficult switchbox and Dense switchbox [Joobani 1986] without inserting any blank row or column (Figures 24(a) and 24(b)). As the complexity is linear in the area, the algorithm terminates very fast. For both these benchmark examples, no call to the maze router (as in Step 3(d)(iii) of Algorithm MD-SU) is necessary. The results are summarized in Tables V and VI. These results show significantly low via count and reduced wire length, thus establishing the superiority of the proposed router to others based on classical strategies.

Table VI. Comparison of the Number of Vias and Wire Length

Switchbox example	Number of vias		Wire length		
	In[a]	MD methods	In[a]	In[b]	MD methods
Burstein's (Figure 24(a))	39	31	541	545	540.11
Dense (Figure 24(b))	29	26	510	510	494.66

[a]Shin and Sangiovanni-Vincentelli [1986].
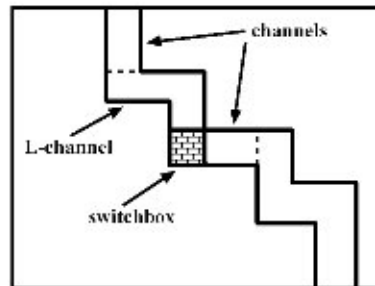[b]Tzeng and Sequin [1988].

Fig. 25. Routing a staircase channel.

7.5 Staircase Routing

A staircase channel is an isothetic rectilinear region monotonically increasing from one side of the floorplan to another side (Figure 25), with terminals along the two rectilinear boundaries except on the top and bottom sides. It was proven [Dai et al. 1985; Sur-Kolay and Bhattacharya 1991] that for any floorplan, there exists a channel definition which induces acyclic ordering of the staircase channels, thereby enabling addition of extra tracks if required, without rerouting the previously routed channels. A monotone staircase routing region is a generalization of L-channels, that is, a concatenation of L-channels. The algorithm to route such a staircase channel is similar to MD-L where the entire staircase is straightened and terminal alignment for each subchannel done to obtain minimum density over the entire channel. However, if the density varies widely along the staircase, it should be subdivided into a series of smaller staircases where for each smaller staircase the densities of the subchannels are more or less uniform. There is scope for minor refinement of routing at a bend where the two subchannels have unequal densities. At the bend (junction) where two consecutive smaller staircases with different densities meet, an instance of switchbox routing is created. This switchbox can then be routed by one of the routers proposed in Section 7.1.

8. CONCLUSION

A unified routing scheme based on the Manhattan-diagonal model is reported for routing regions such as straight channels, L-channels, switchboxes, and staircases. These regions may appear especially in nonslicing floorplans. The scheme is also useful for general non-Manhattan area routing and multichip modules (MCM). The proposed algorithms are simple, terminate in time linear

in the routing area, and provide elegant solutions to complex routing problems. As the MD model has an extended set of design rules, the implications of a gridless routing approach for this model need to be addressed.

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