M.Tech. (Computer Science) Dissertation Series

Tree-Based Hybrid Scan Architecture for VLSI Testing

A dissertation submitted in partial fulfillment of the requirements for the M.Tech. (Computer Science) degree of the Indian Statistical Institute

By

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Synopsis: “Tree-Based Hybrid Scan Architecture for VLSI Testing”

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Motivation:

The important issues and challenges of scan-based testing are

- ***Test application time constraints:*** The objective is to reduce test application time due to scan operations. Reducing the test application time is one of the critical factors to reduce the test cost for a scan circuit.
- ***Power/energy minimization:*** It has important role in the context of deep sub-micron technology because of higher device densities and clock rates.
- ***Number of test vectors:*** Selection of fewer number of test vectors without degrading the fault coverage.

Most design-for-testability (DFT) techniques deal with either the resynthesis of an existing design or the addition of extra hardware to the design. Most approaches require circuit modifications and affect such factors as area, I/O pins, and circuit delay. The values of these attributes usually increase when DFT techniques are employed. Hence, a critical balance exists between the amount of DFT to use and the gain achieved.

Test complexity includes the complexity of test generation and algorithms for constructing a test for a complex circuit. Test complexity can be converted into costs associated with testing process. There are several facets to this cost, such as cost of test pattern generation, storing test pattern, the cost of fault simulation and generation of fault location information, the cost of test equipment, and the cost related to the testing process itself, namely the time required to detect and/or isolate a fault. Because these costs can be high and may even exceed design costs, it is important that they be kept within reasonable bounds.

Till date there is no such circuit independent and test vector set independent architectural approach, which handles satisfactorily the key issues such as test application time reduction, power/energy minimization, test vector number reduction with simplified hardware modification yielding high fault coverage.

Problem definition:

As we stated earlier, although the full-scan method reduces the cost of test generation and provides high fault coverage, but the inherent serial nature of scan path increases the test application time and energy consumption in test mode significantly. The number of clock cycles needed to scan in/out the test data is equal to the product of number of test patterns and the length of the scan chain. Hence we have concentrated on the fact that the test application time (also the test data volume) and consequently the usage cost of the automatic test equipment, can be lessened either by reducing the number of test patterns or by shortening the scan chain length as used in tree based scan architecture.

Our Contribution:

In this thesis, a novel two-stage hybrid DFT approach is proposed that drastically reduces the scan-shift and clock activity during testing. The design is independent of the structure of the circuit-under-test (CUT) or its test set. A tree-type structure is employed for designing the scan architecture, incorporating very simplified hardware circuitry. It provides a significant reduction both in instaneous and average power needed for clocking and scan shifting. It reduces the number of test vectors compared to autoscan technique.

The proposed scheme:

Objective:

Our goal is to introduce a power/energy minimized technique which can be obtained reordering the test vector set and introducing a tree-type-interconnection of flip-flops in test mode or scan mode. In our work we also reduce the number of scan test vectors (i.e. the vectors that are set in the inputs of the circuit in test mode) at the cost of adding some internally generated responses. The design is independent of the structure of CUT .

Scheme Overview

The proposed architecture is two-stage hybrid Design:

- Scan tree test mode with circulated responses (STTMCR)
- Linear scan test mode with circulated responses (LSTMCR)

The ***Scan tree testing mode (STTMCR)*** is highly beneficial in power/energy minimization. A significant component of the power consumed in CMOS circuit is caused by the switching activity (SA) at various circuit nodes during operation. The dynamic power consumed at a

circuit node is proportional to the total number of 0 -> 1 and 1 -> 0 transitions that the logic signal undergoes at that node multiplied by its capacitance and the frequency of operation.

The tree architecture in Scan tree mode is motivated by observation that in typical designs with large number of scan flip flops, a major component of energy is consumed in scan-shifting and clocking of the scan chain. In the scan tree mode, flip-flops are oriented in an tree-type structure. Since we focus attention on designs with a single scan input, obviously the scan input is connected to the root of the binary tree. The following properties are desirable in designing such a scan-path and its associated shift control mechanism.

1. It should be possible to load or unload the scan-path with f FFs in $\lceil \log(f) \rceil$ shift clock cycles.
2. It should be possible to completely overlap the loading of a new test vector with unloading of the previous response.
3. It reduces the number of scan test vectors by utilizing internally generated responses as test vectors.

Once the scan test vector is added, the circuit is switched to functional mode and simulates the circuit against the scan vector. On applying a scan test vector, the response stored in the flip-flops is applied, directly to pseudo primary inputs of the CUT at the next clock; an LFSR is used to generate pseudo-random patterns for the primary inputs. In this way, the next test vector is applied. Since these vectors involve the circulation of responses we call then circulating test vectors. These vectors can be applied on a test per clock basis and this saves a lot of time. The circulating vectors will detect transition faults. Circulating vectors work in functional mode, i.e. they perform under fast system clock where as scan vectors are guided by comparatively slow system clock in test mode. We continue to circulate the response it detects new faults. When the current circulating test vector fails to detect any new fault among the remaining faults, the circulation of response is stopped. This is because experimental results show that even if we continue the circulation of response it hardly detects any new fault. Then the next scan test vector is selected for initiating next circulation.

The ***Linear Scan test mode with circulated responses (LSTMCR)*** is used because the scan tree mode sometimes yields poor fault coverage. To cover the remaining hard-to-detect (HTD) faults a few test vectors are chosen from the original test set for application in the serial mode. Again we used output response circulation to reduce the cost response analysis.

The idea is to apply the majority of test vectors in Scan tree mode (STTMCR) and few in Linear Scan mode (LSTMCR). Switching of modes can be implemented by a controller, which consists of some logic and a counter that counts the number of test patterns to be applied in each mode.

Experimental Results:

Result is illustrated in Table 1.

Circuit Name	Number of flip-flops (*f*)	Number of scan test vec. generated by ATALANTA (*y*)	# scan shifts (*y * f*)	Number of scan test vectors		Number of Circular Test vectors	# scan shifts in proposed approach (a)	% reduction in the number of scan vec(z)	% reduction in the number of scan shift(w)	Total faults	% Fault coverage
				STTMCR (y1)	LSTMCR (y2)						
S298	14	31	434	5	20	18	300	19	31	308	100
S344	15	24	360	7	10	16	178	29	51	342	100
S386	6	71	426	11	46	21	309	20	28	384	100
S953	29	95	2755	15	72	31	1947	9	29	1079	100
S1196	18	139	2502	67	-	103	335	59	87	1242	100
S1238	18	150	2700	59	1	57	313	60	88	1355	95
S1423	74	62	4588	9	40	56	3023	21	34	1515	99.076
S1488	6	127	762	16	75	48	498	29	35	1486	100
S1494	6	126	756	12	55	77	366	47	52	1506	99.203
S15850.1	534	443	236562	34	350	160	187240	14	21	11725	96.682
S35932	1728	65	112320	8	15	51	26008	65	77	39094	89.804

Table 1: Comparison of test vectors generated by ATALANTA and by the proposed approach on specified benchmark Circuit ISCAS-89

The column 3 indicates the number of test vectors generated by ATALANTA .The column 5 and column 6 include the number of scan test vectors and column 7, the circular vectors generated by the proposed approach, yielding the same fault coverage as the tool ATALANTA. Column 9 indicates the percentile reduction in the number of scan vectors and evaluated as $z = (y - y1 - y2) / y * 100$ where f is the number of flip-flops of the circuit. Column 10, illustrates the percentile reduction in the number of scan shifts and evaluated as $w = ((y * f - y1 * \lceil \log(f) \rceil - y2 * f) / (y * f)) * 100$. Column 4 an 8 shows the no of clock pulse needed for shifting in test mode by ATALANTA and the proposed approach respectively.

Conclusion:

A new circuit independent and test set independent hybrid test architecture is described here and empirically evaluated, which shows improvement in test application time and power/energy consumption reduction.

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Certificate of Approval

This is to certify that this dissertation thesis titled "Tree-Based Hybrid Scan Architecture for VLSI Testing" submitted by Mr. Subhra Lahiri, in partial fulfillment of the requirements for the M. Tech. (Computer Science) degree of the Indian Statistical Institute, Kolkata, embodies the work done under my supervision.

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Abstract:

Full scan based design technique is widely used to alleviate the complexity of test generation for sequential circuits. However, this approach leads to substantial increase in the test application time, because of serial loading of test vectors, especially in today's digital circuit containing thousands of flip-flops. In a scan-based system with a large number of flip-flops, a major component of power is consumed during scan-shift and clock operation in test mode. In this thesis, a novel two-stage hybrid DFT approach is proposed that drastically reduces the scan-shift and clock activity during testing. The design is independent of the structure of the circuit-under-test (CUT) or its test set. A tree-type structure is employed to design the scan architecture incorporating very simplified hardware circuitry. It provides a significant reduction both in instaneous and average power needed for clocking and scan shifting. It reduces the number of test vectors compared to autoscan technique. The test suite consists of: (i) some externally deterministic test vectors to be scanned in where flip-flops are oriented in tree-type structure, (ii) internally generated responses of the CUT to be re-applied as tests iteratively, in non-scan mode, (iii) a set of externally deterministic test vectors to be scanned in where flip-flop are interconnected in linear scan chain. The method uses only combinational ATPG for deterministic testing and thus makes a good use of scan based and non-scan testing. Experimental results on ISCAS-89 benchmark circuits reveal a significant reduction of test application time and energy/power reduction due to shift in test mode.The architecture fits well to built-in self-test (BIST) scheme.

Keywords *– Full scan, test application time, DFT, energy/power reduction, ISCAS-89*

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Chapter 1

Introduction

1.1 Design for Testability (DFT):

Need for VLSI Testing:

A VLSI chip is manufactured through a series of steps that involve chemical, metallurgical and optical processes. If the yield of good chips is 75%, then on an average 25% of manufactured chips will be faulty. Thus at the end of the VLSI manufacturing process we always have “testing”, which isolates the good chips from bad ones. Inadequate testing will have some faulty chips shipped to the customer. At the same time, the cost of testing directly increases the overall cost of chips.

Digital Design for Testing (DFT) and Scan Design Overview:

For a VLSI chip to be manufactured, we must have a verified design and a set of tests. The following questions characterize testing of complex systems:

- Can tests that detect all faults to be assured?
- Can test development time be kept low enough to be economical?
- Can test execution time be kept low enough to be commercial?

Design for testability (DFT) refers to those design practices that allow us to answer the above questions in affirmative. We will focus on DFT techniques that aim at improving the testability of stuck-at faults.
Logic DFT is of two types

- Ad-hoc DFT
- Structured DFT

The ad-hoc DFT: It relies on good design practices learned from experience. Some of these are:

- Avoid asynchronous logic feedbacks.
- Make flip-flops initializable.
- Avoid gates with large number of fan-in signals.
- Provide test control for difficult to control signals

Unfortunately ad-hoc DFT is discouraged for large circuits.

The structured DFT: As the size and the complexity of digital systems grew it becomes popular. Here extra logic and signals are added to the circuit so as to allow the test according to some predefined procedure. Apart from the normal functional mode, such a design will have one or more test modes. Commonly used structured methods are scan and built-in self-test.

Scan Design: The main idea of the scan design is to obtain control and observability of for flip-flops. This is done by adding a test mode to the circuit such that when a circuit is in this mode, all flip-flops functionally form one or more shift registers. The inputs and outputs of these shift registers are made into primary inputs and outputs. Thus, using the test mode, all the flip-flops can be set to any desired states by shifting those logic states into the shift register. Similarly,
The states of flip-flops are observed by shifting the contents of scan register out. All the flip-flops can be set or observed in a time (in terms of clock periods) that equals to the number of flip-flops in the longest scan register. In practice, however, a design can have any number of scan registers.

A simple example of *scan design*:

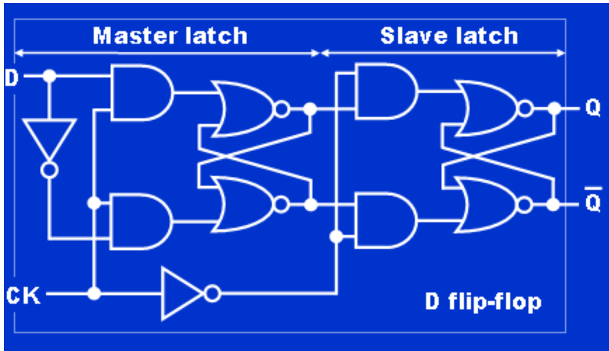

Figure 1.1 – a DFF

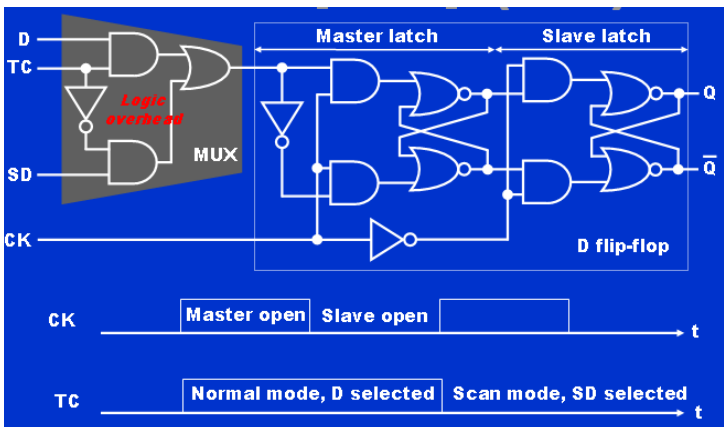

Figure 1.2: A SFF

For a circuit to have scan capability, first the D type flip-flops (DFF) (referred in Figure 1.1) with one clock signal is used, all of which are controlled from primary inputs. Once the circuit is functionally verified, the DFFs are replaced by scan flip-flops (SFF) (referred in Figure 1.2). Here a multiplexer and two new signals, scan-data SD and test control TC, are added to D flip-flop (DFF).The original data input D is stored in the flip-flop when TC is 1 and SD is stored when TC is 0.

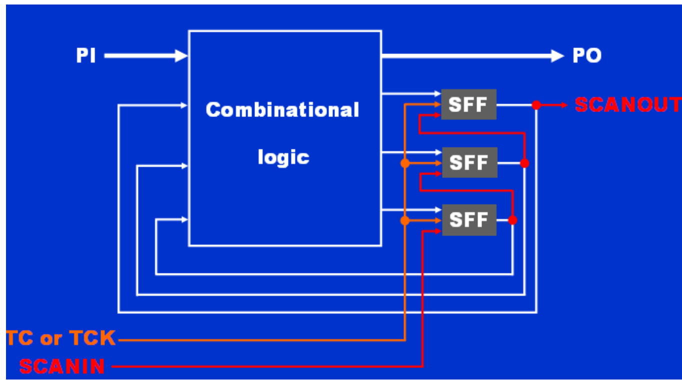

Figure 1.3: A scan design schematic

1.2 Common Scan Architectures and Methodologies:

1.2.1 Full-scan methodologies:

Full scan based design technique is widely used to alleviate the complexity of the test generation for sequential circuits. It transforms a sequential circuit into its combinational parts in the test mode. However, this approach leads to substantial increase in test application time, because serial loading of vectors, especially in today's digital circuit containing thousands of flip-flops. In a scan-based system with a large number of flip-flops, a major component of power is consumed during scan shift and clocking operation in test mode. Regarding test methods, deterministic testing using ATE provides high fault coverage. Figure 1.3 shows a scan design schematic view.

1.2.2. Illinois Scan Architecture:

It consists of two modes of operation. The top part of the figure shows a regular scan chain, which is known as Serial mode. The bottom part of the figure shows the scan chain broken up into segments, called the Broadcast mode. Here the scan-in pin that originally went into the entire scan chain now feeds into each of the scan chain segments. Thus each segment will be inputted the same data in parallel. However, this is limited to testing several independent

circuits in parallel. The outputs of the scan chains are compressed into a multiple input signature register (MISR). Figure 1.4 illustrates this architecture.

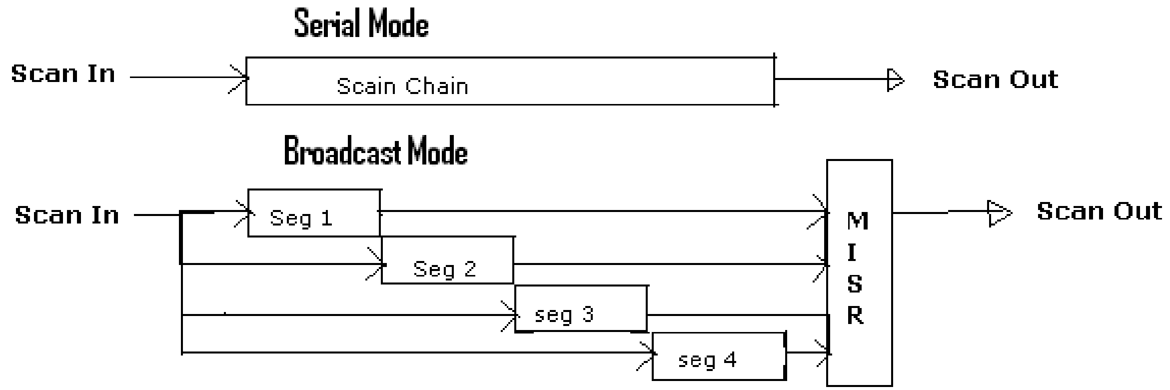

Figure 1. 4: Two Modes of Illinois Scan Architecture

1.2.3. Tree-based Scan path Architecture:

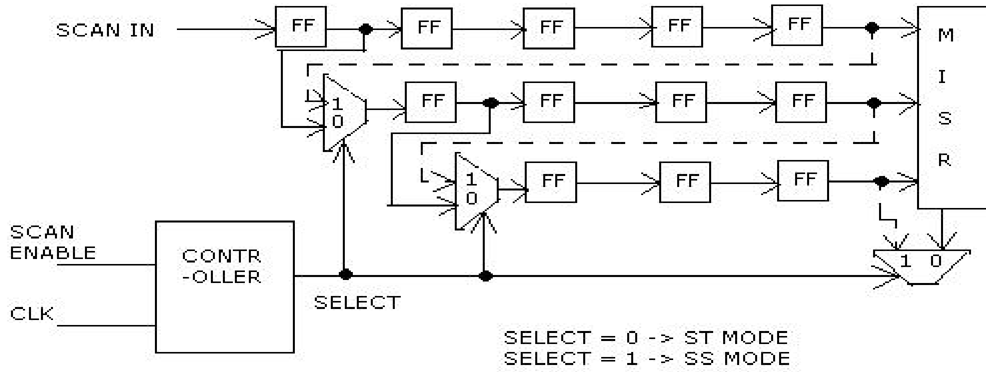

Figure 1. 5: Scan tree architecture with dynamic reconfiguration

Tree-based scan path architectures have recently been suggested for reducing test application time or test data volume in today's high-density very large scale integration circuits. However, these techniques strongly rely on the existence of a large number of compatible sets of flip-flops under the given test set and therefore may not be suitable for highly compact test set generated by efficient ATPG tools. Tree based architectures also suffer from loss of fault

coverage while achieving a significant reduction ratio for test time and data. Tree based scan architecture is shown in Figure 1.5.

1.2.4. Autoscan Architecture:

Autoscan is a design-for-testability technique for synchronous sequential circuits. Autoscan uses scan chains similar to conventional scan. However it gives up the external scan inputs and outputs in order to eliminate the test data volume associated with them. Scan operations under autoscan improve the circuit testability by allowing the circuit state to be modified through shifting. Due to removal of the scan inputs and outputs, synthesis of the scan chains under autoscan does not have to satisfy all the constraints imposed by conventional scan chains. Figure 1.6 shows the autoscan architecture for S27.

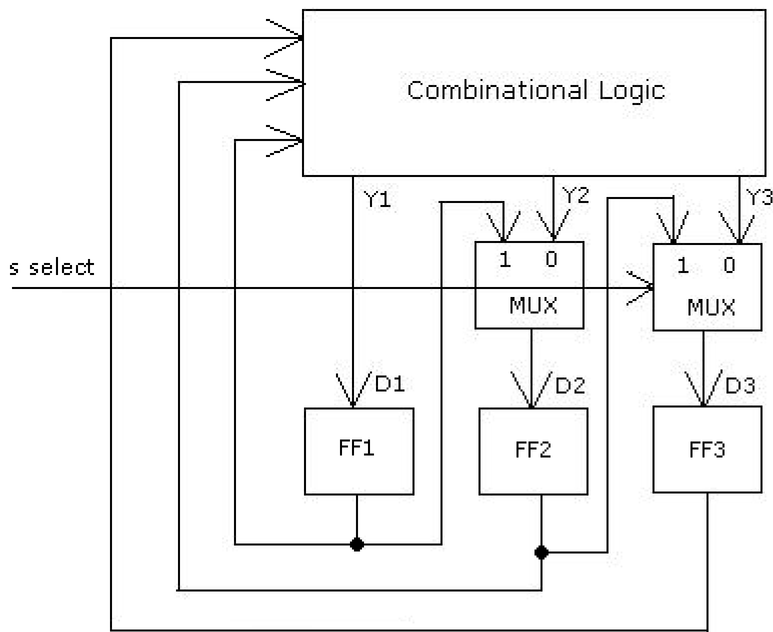

Figure 1. 6: Circuit Configuration for S27

1.3. Issues and Challenges:

Here we mention the important issues and challenges of Scan Based Testing.

- ***Test Application time constraints:*** The objective is to reduce test application time due to scan operations. Reducing the test application time is one of the critical factors to reduce the test cost for a scan circuit.
- ***Power/energy minimization:*** It has important role in the context of deep sub-micron technology because of higher device densities and clock rates.
- ***Number of Test vectors:*** Selection of fewer number of test vectors without degrading the fault-coverage.

Chapter 2

Scan Based Design for Testability (DFT)

2.1 Preliminaries:

Test complexity includes the complexity of test generation and algorithms for constructing a test for a complex circuit. Test complexity can be converted into costs associated with testing process. There are several facets to this cost, such as cost of test pattern generation, storing test pattern, the cost of fault simulation and generation of fault location information, the cost of test equipment, and the cost related to the testing process itself, namely the time required to detect and/or isolate a fault. Because these costs can be high and may even exceed design costs, it is important that they be kept within reasonable bounds.

Controllability, observability and predictability are the most important factors that determine the complexity of deriving a test of the circuit. The objective of any DFT technique is to improve those factors.

2.2 Trade-Offs

Most DFT techniques deal with either the resynthesis of an existing design or the addition of extra hardware to the design. Most approaches require circuit modifications and affect such factors as area, I/O pins, and circuit delay. The values of these attributes usually increase

when DFT techniques are employed. Hence, a critical balance exists between the amount of DFT to use and the gain achieved.

2.3 Problem formulation

As we have already told, although the full-scan method reduces the cost of test generation and provides high fault coverage, but the inherent serial nature of scan path increases the test application time and energy consumption in test mode significantly. The number of clock cycles needed to scan in/out the test data is equal to the product of number of test patterns and the length of the scan chain. Hence we have concentrated the fact that the test application time (also the test data volume) and consequently the usage cost of the automatic test equipment, can be lessened either by reducing the number of test patterns or by shortening the scan chain length as used in tree based scan architecture.

2.4 Previous Work:

Janak H. Patel et al. in [1] and [2] describes a scan architecture which is popularly known as Illinois Scan Architecture introduces Parallel Serial Full Scan (Multiple Scan Chain), for reducing the test application time. It yields low fault coverage and partially dependent on flip-flop compatibility. So this scan architecture is not circuit as well as test set independent.

Bhargab B. Bhattacharya et al. in [3] give a test set independent Double tree Scan Architecture which is not at all circuit independent if the number of flip-flops in the circuit is not in the power of two. It includes some additional hardware cost also.

Irith Pomeranz and Sudhakakar M. Reddy in [4] introduce a circuit independent Autoscan technique. In true sense it is not fully independent of test vector set. It costs a huge number of iteration before converging.

Banerjee et al. in [5] gives a Scan Tree Technique which strongly rely on the existence of a large number of compatible sets of flip-flop under the given test set generated by an efficient ATPG tool. The method is suitable for highly compact test set having fewer don't cares and low compatibility.

2.5 Our Contribution

In this thesis, a novel two-stage " tree-based hybrid Design-For-Testability " approach is proposed that drastically reduces the scan-shift and clock activity during testing. The design is independent of the structure of the circuit-under-test (CUT) or its test set. The tree-type structure of moderate height is employed to design the scan architecture incorporating very simplified hardware circuitry. It provides a significant reduction both in instaneous and average power needed for clocking and scan shifting. It reduces the number of test vectors compared to autoscan technique.

Chapter 3

The proposed scheme

3.1 Objective

Our goal is to introduce a power/energy minimized technique which can be obtained reordering the test vector set and introducing a tree type interconnection of flip-flops in test mode or scan mode. In our work we also reduce the number of scan test vectors (i.e. the vectors that are set in the inputs of the circuit in test mode) at the cost of adding some internally generated responses. The design is independent of the structure of CUT and its test set.

3.2 Scheme Overview

The proposed architecture is two-stage hybrid Design.

- Scan tree test mode with circulated responses (STTMCR)
- Linear scan test mode with circulated responses (LSTMCR)

The ***Scan tree mode (STTMCR)*** is highly beneficial in power/energy minimization. A significant component of the power consumed in CMOS circuit is caused by the switching activity (SA) at various circuit nodes during operation. The dynamic power consumed at a circuit node is proportional to the total number of 0 -> 1 and 1 -> 0 transitions that the logic signal undergoes at that node multiplied by its capacitance and the frequency of operation.

The tree architecture in Scan tree mode (STTMCR) is motivated by observation that in typical designs with large number of scan flip flops, a major component of energy is consumed in scan-shifting and clocking of the scan chain. In the scan tree mode flip-flops are oriented in an arbitrary height-balanced binary tree fashion. Since we focus attention on designs with a single serial scan input, obviously the scan input is connected with the root of the binary tree. The following properties are desirable in designing such a scan-path and its associated shift control mechanism.

1. It should be possible to load or unload the scan-path with f FFs in $\lceil \log(f) \rceil$ shift clock cycles.
2. It should be possible to completely overlap the loading of a new test vector with unloading of the previous response.
3. It reduces the number of scan test vectors by utilizing internally generated responses.

Once the scan test vector is added, the circuit is switched to functional mode and simulates the circuit against the scan vector. On applying a scan test vector, the response stored in the flip-flops is applied, directly to pseudo primary inputs of the CUT, at the next clock; an LFSR is used to generate pseudo-random patterns for the primary inputs. In this way, the next test vector is applied. Since these vectors involve the circulation of responses we call then circulating test vectors. These vectors can be applied on a test per clock basis and this saves a lot of time.

The circulating vectors will detect transition faults. Circulating vectors work in functional mode, i.e. they perform under fast system clock where as scan vectors are guided by comparatively slow system clock in test mode.

We continue to circulate the response till it detects new faults. When the current circulating test vector fails to detect any new fault among the remaining faults, the circulation of response is stopped. This is because experimental results show that even if we continue the circulation of response it hardly detects any new fault. Then the next scan test vector is selected for initiating next circulation.

The ***Linear Scan test mode with circulated responses (LSTMCR)*** is used because the scan tree mode sometimes yields poor fault coverage. To cover the remaining hard-to-detect (HTD) faults a few test vectors are chosen from the original test set for application in the serial mode. Again we used output response circulation to reduce the cost response analysis.

The idea is to apply the majority of test vectors in Scan tree mode (STTMCR) and few in Linear Scan mode (LSTMCR). Switching of modes can be implemented by a controller, which consists of some logic and a counter that counts the number of test patterns to be applied in each mode.

3.3 Motivating example

In this section the basic procedure is illustrated using a small example. Let us consider the ISCAS89 benchmark circuit s1196, which has 14 primary inputs, 14 primary inputs, 18 D type flip-flops, 141 inverters and 388 gates. In this circuit 1242 number of stuck-at faults can be possible.

The number of test patterns generated by ***ATALANTA*** for combinational part (i.e. considering the inputs to the flip-flops as pseudo primary outputs and the outputs of the flip-flops as pseudo primary inputs) of this circuit is 139, which yields 100% fault coverage (illustrated in Table 3.1).

Circuit name	Number of Test Vector	Fault Coverage
S1196	139	100%

Table 3.1: Test Detail by ATALANTA on s1196

Here we need to scan in all the test vectors and observe their corresponding outputs after each functional clock cycle that requires again the scan out of the pseudo-primary response.

On the other hand ***the proposed approach*** (ref. Table 3.2) gives 67 scan vectors and 103 circulating vectors and yield 100% fault coverage. Thus we reduce the number of scan vectors at the cost of adding some internally generated response. In case of applying circulating vector we utilize the part of the response stored in the flip-flops thus avoids the time consuming scan in process.

Circuit name	Scan Tree Mode			Linear Scan Mode			Total faults	Fault Coverage
	SV	CV	UF	SV	CV	UF		
S1196	67	103	0	-	-	-	1242	100%

Table 3.2: Test Detail by the proposed Approach

SV –Scan Vector, CV- Circulating, UF- Undetected Fault

So the proposed approach is highly rich in observability point of view. Here observability is 50% better than the naïve approach.

3.4 The proposed test architecture

The overall architecture of this testing scheme is given in figure 3.1.We load the flip-flops (which forms the tree-type interconnection is shown in Figure 3.2) in scan-tree mode using scan-in pin connected at root. We scan out the response stored in the flip-flops after a single circulation sequence and simultaneously scan in the next test vector for the next sequence. Thus a compressed signature of the initial scan test vector and its subsequent sequence of circulation of response is scanned out at the end of every sequence. We also compress the primary outputs using a MISR scanning out the signature only during the scan out process, which allows to circulate the response of the CUT (Circuit under test) at the normal speed, which in turn expedite the testing process heavily. In Linear scan test mode flip-flops are configured in linear scan chain as illustrated in Figure 3.3.

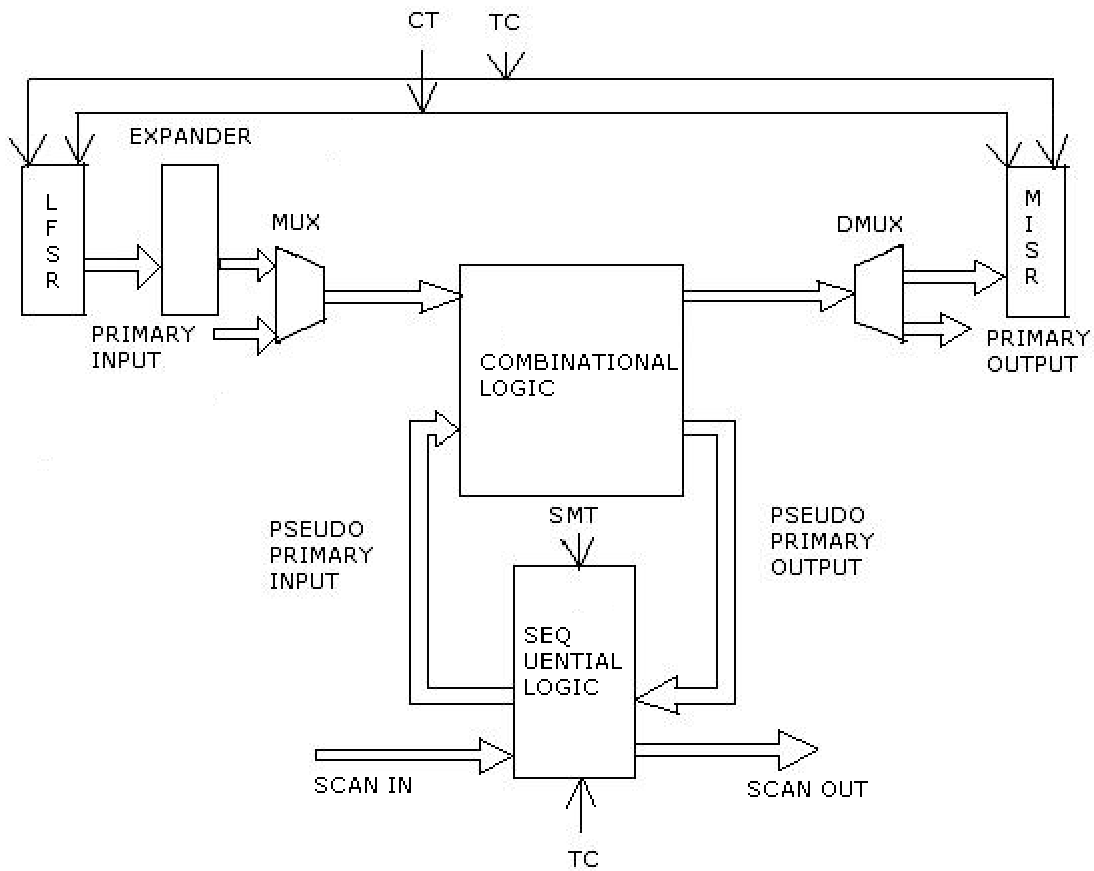

Figure 3.1: Proposed test architecture

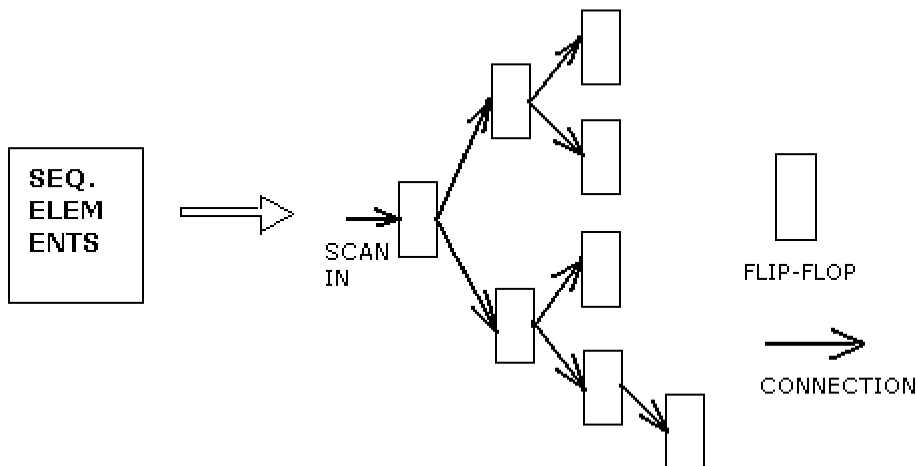

Figure 3.2: Orientation of flip-flops in Scan Tree mode (STTMCR)

(The circuit contains 8 flip-flops in the example)

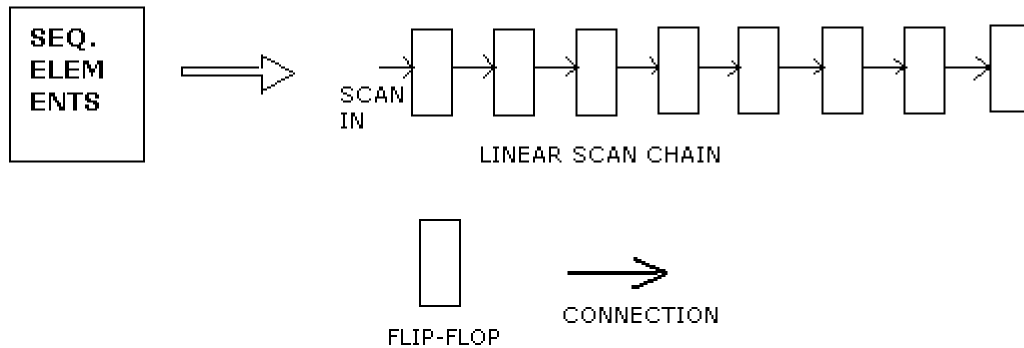

Figure 3.3: Orientation of flip-flops in Linear Scan Test mode (LSTMCR)
(The circuit contains 8 flip-flops in the example)

The proposed architecture consists of two stages; scan tree test mode (STTMCR) and linear scan test mode (LSTMCR). Each of these stages again contains three modes, *viz.* ***normal mode, scan mode and circulating response mode***. In the ***normal mode*** the circuit operates according to its functional specification. In the ***scan mode*** the test is shifted either in scan-tree or in scan chain depending on the configuration and the response is stored in the scan chain and is shifted out as well. In the ***circulating response mode***, we apply the pseudorandom pattern generated by LFSR to the primary inputs of for testing. In this mode only LFSR will be activated while the flip-flops will behave as in the normal mode. Scan shift operation does not take place in this mode.

Since the number of primary inputs can be of the order of hundreds, an expander is used to provide pseudorandom patterns to a large number of primary input lines using a small LFSR. The logic of the expander circuit is very simple. Every output line of the expander circuit is driven by a XOR gate. The inputs of the XOR gate are connected to the output of a randomly chosen flip flop. Figure 3.4 shows an example of the expander where two input XOR gates are used. A multiplexer is used to select between the input from LFSR and the external input that comes from the input pins.

Using three input lines TC, CT and SMT, the two stages and three modes in each stage can be implemented. During the normal mode of operation of operation both the TC and CT are kept at 0 and SMT is kept as don't care condition. In the scan mode in STTMCR (scan tree) stage TC is kept at 1 and SMT is kept at 0, the flip flops forms a tree-type structure and shift in shift out operation take place. On the other hand in the scan mode of the LSTMCR (Linear scan) stage SMT is set at 1 and TC is kept at 1, the flip-flops form a scan chain, and shift in shift out operation take place. The inputs to the flip-flops come from the combinational part of the circuit when TC is 0. In circulating response mode CT and TC are held at logic 1 and logic 0 respectively. In this mode LFSR gets activated and primary inputs are driven using the pseudorandom pattern for the next circulating vector is generated. The initial state of the LFSR is loaded during scan mode.

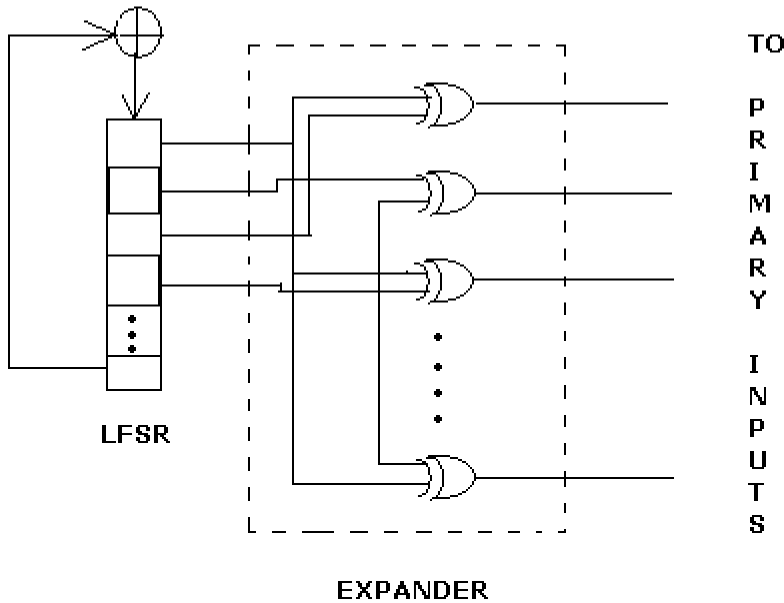

Figure 3.4: Schematic Diagram of expander

Mode of operation	TC	CT	SMT
Normal	0	0	X
Scan test in Scan Tree (STTMCR) stage	1	0	0
Scan test in Linear Scan(LSTMCR) stage	1	0	1
Circulating Response	0	1	X

Table 3.3: Modes of Testing

The CT line also controls the multiplexer. In normal mode of operation the multiplexer allows the primary input to come directly from the input pins, whereas in circulating test mode of operation the primary input is driven by the output of the expander. In the scan mode neither does the primary input has any effect on the state of the flip-flops, nor do the patterns corresponding to the primary input participate in testing. However during the scan mode CT is kept at 0. The demultiplexer is controlled in a similar way.

A Multiple Input Signature Register (MISR) is added to compress the primary output values. A scan test vector and its sequence of circulated responses are applied and the corresponding primary output patterns are compressed into the MISR and compressed signature is observed before the application of the next scan test vector.

Chapter 4

Implementation Details and Performance Evaluation

4.1 Implementation Details:

The objective of our simulator is to generate ***TEST VECTOR.*** We incorporate a heuristic approach to generate optimal resultant test set. Our objective is to reduce the number of scan vectors at the cost of in circulating vectors. We have two modes of operation scan tree mode (STTMCR) and linear scan mode (LSTMCR), the detail implementation steps of each stage is explained bellow:

Step 1: Generation of bipartite graph

A bipartite graph $G = \{V, E\}$ where V is set of vertices and E is the set of edges. Let T represents the test vectors; F represents the set of faults. The initial test vector set is obtained by the tool ATALANTA. Now T and F are the two independent sets of graph G. Hence $T \cup F = V$ and $T \cap F = \Phi$. Each edge $e_{ij} \in E$ between vertex $t_i \in T$ and $f_j \in F$ indicates that vector t_i detects the fault f_j.

Procedure Bipartite_graph_generation

Initialize the degrees of all $v_i \in V$ to 0;

For each test vector $t_i \in T$ ***do***

  For each fault $f_j \in F$ ***do***

    Perform concurrent fault simulation;

    If t_i detects f_j

      Create an edge e_{ij} between t_i and f_j

    End if

  End for

End for

Step 2: Test Vector generation in scan tree mode (STTMCR)

Step2.1 Scan test vector generation:

Through scan-in push an arbitrary test vector of bits 0/1 s of length equal to height of the tree in the direction from root to leaves so that the flip-flops of same level contains the same value.

We follow a heuristic approach in selection of test vectors. Consider the test vector set generated by ATALANTA (and name it TA) and calculate the hamming distance (HD) between the generated pseudo-primary input vector and the pseudo-primary input vectors of TA. Then mark all the test vectors of TA whose HD are within a certain threshold. Then sort the marked test vectors in decreasing order according to the number of fault detection. Then choose the primary inputs from the primary input of sorted test sequence one by one. If that applied test vector gives desired fault coverage then commit the action and delete the detected faults from the fault list of bipartite graph. Otherwise select the next test vector of the sorted list. After the exhaustion of the sorted list we starts generating pseudo random primary inputs and simulate that.

Step 2.2 Circulating test vector generation:

We have already told the greedy approach of selecting scan test vectors. Fault simulation is done to compute which faults are detected by the current test vector. The detected faults are dropped with the entire edges incident on the fault vertices. The response is composed of two parts, viz. the primary output part and another part, called pseudo primary outputs, and stored in the flip the flip-flops. Normal approach for scan based approach for scan based testing is to verify the primary output, and shift out the values stored in the flip-flops as well as shift in the next vector.

In the proposed approach, we use the part of response of a scanned test vector that is stored in the flip-flops, as the pseudo primary input of the next vectors. The primary inputs are set using an LFSR. In this way we perform the circulation of the response. The faults that are detected by the circulation are dropped and the corresponding edges in the bipartite graph are deleted. The subsequent circulations of the responses are continued till the circulation is able to detect new faults.

It is observed that even if a particular circulation fails to detect any new fault, the next circulation may detect new faults. Thus we circulate the response for a particular number and if the sequence fails to detect any new fault we select the next scan test vector. It is also found from experimental results that the improvement depends on the sequence length and significant improvement can be achieved for large circuits.

Procedure Test_vector_set_generation

Input: Bipartite graph (test vector vs. fault) and sequence length.

Output: A set of scan test vectors and the subsequent circulation vectors for each scan test vectors.

```
While Current fault coverage < desired coverage
Do
    Scan in an arbitrary random vector in flip-flops oriented in tree fashion;
    STV is equal to1;
    Repeat
        Calculate the hamming distance between the input and pseudo-primary
        input of initial test set;
        Sort them in decreasing order of hamming distance value which
        satisfy a certain threshold value;
        Select the available best test vector from the sorted set and set its
        primary input as the primary input of scan test vector;
        If sorted test set exhausted
            Generate a random vector for primary input of scan test vector
            using LFSR;
        End if

        STV is equal to zero;
        Run the concurrent fault simulator;
        Mark the detected faults;
         Drop the detected fault and its associated edges;
        Remove zero out degree test vectors of the bipartite graph;

          If  STV=0;
                Set the pseudo primary inputs of the response of the last vector;
        End if

     Until a sequence of circulating vectors fails to detect a new fault;

End While
```

Step 3: Test Vector generation in linear scan test mode (LSTMCR)

It is more or less same as the step 2 stated earlier except the fact that here flip-flops form a scan chain. While selecting the scan vector the pseudo primary input shift in shift out of bit operation takes place through linear scan chain.

4.2 Performance evaluation:

Let's assume that for a particular circuit there is v number of test vectors generated by ATALANTA to achieve certain fault coverage. To meet the same fault coverage the proposed approach needs vs_1 number of scan vectors in scan-tree mode (STTMCR) and vs_2 number of scan vectors in linear-scan mode and vc number of circulating test vectors.

Assume that the circuit contains n number of flip-flops. As we know for testing mode we use comparatively slower system clock than functional mode. We also assume that testing mode, functional mode clock pulse are of t_t and t_f time units respectively.

Application time reduction:

In the first case we need to need to scan in the pseudo primary input of each of the v test vectors in the flip-flops (oriented in linear scan chain) through shifting in/out. For each test vectors it needs n clock pulse (each pulse of t_t duration) resulting $n * t_t$ time unit. After each clock pulse the pseudo primary response is needed to scan out through shifting and new pseudo primary output is needed to scan in. So the procedure takes in total $n * v$ number of clock pulses in test mode resulting $n * t_t * v$ time unit. Time consumed in functional mode is the multiplication of number of test vectors v and clock pulse t_f, so $v * t_f$ unit time. So the total time needed is $(n * t_t + t_f) * v$ time unit.

On the other hand, in the proposed approach the scan-tree mode (STTMCR) has vs_1 number of scan vectors. Each scan vector is required to scan in through the n flip-flops oriented in height balanced binary tree, which takes $\lceil \log(n) \rceil$ clock pulses in test mode. So for vs_1 number of scan vectors needed to be scan out and simultaneous scan in except the first and last one.

So total time needed in STTMCR mode is $(vs_1 - 2) * \lceil \log(n) \rceil$ clock cycles in test mode, so $vs_1 * \lceil \log(n) \rceil * t_t$ time unit (eliminating 2 to make the calculation easier).Time consumed by vs_1 number of scan vectors in functional mode is $vs_1 * t_f$ time unit. So in total vs_1 number of scan vectors consumes $(\lceil \log(n) \rceil * t_t + t_f) * vs_1$ time unit.

In linear scan mode there are vs_2 number of scan vectors. The pseudo primary input of each vector requires to scan in through n flip-flops oriented in linear scan chain, and pseudo primary output needs to scan out by shifting out. Though except first and last case the scan in and scan out process are overlapping. It takes $vs_2 * n * t_t$ time unit in test mode $vs_2 * t_f$ time unit in functional mode, so it takes $(n * t_t + t_f) * vs_2$ time unit .

Since there are vc number of circulating vector works in functional mode so it consumes $vc * t_f$ time unit.

The proposed approach totally takes $(\lceil \log(n) \rceil * t_t + t_f) * vs_1 + (n * t_t + t_f) * vs_2 + vc * t_f$ unit time where as the ATALANTA guided method takes $(n * t_t + t_f) * v$ unit time.

Proposed approach is beneficial in application time point of view iff,

$$\{ (\lceil \log(n) \rceil * t_t + t_f) * vs_1 + (n * t_t + t_f) * vs_2 + vc * t_f \} > \{ (n * t_t + t_f) * v \}$$

Assuming $t_t = 1.5 * t_f$, our experimental shows that most of the cases our algorithm is giving better result.

Power/energy minimization *:*

As we have already told that the dynamic power consumed at a circuit node is proportional to the total number of 0 -> and 1 -> 0 transitions. The number of shifts in ATALANTA guided linear scan approach is $O(n^2)$ for each test vector, so $v * O(n^2)$ shifts in total.

On the other hand our approach, in Scan tree test mode (STTMCR) takes $O(\log^2 n)$ shifts for each vector, so $O(\log^2 n) * vs_1$ shifts in total. In linear scan test mode (LSTMCR) we need $O(n^2)$ for each test vector, so $vs_2 * O(n^2)$ shifts in total.

Assuming that the probability of bit transition in each shift is equal, we conclude that power/energy consumption is proportional to the number of shifts.

Our approach is beneficial for in energy/power with respect to scan shift iff

$$\{ O(\log^2 n) * vs_1 + O(n^2) * vs_2 \} > \{ O(n^2) * v \}$$

Experimental results favour our approach.

Chapter 5

Experimental Results

The tool ATALANTA and HOPE are used in the experiment. The ATALANTA is needed to generate the test patterns for the experiment. This tool generates test patterns for combinational part (available as ISCAS-89 SCAN circuits) of the ISCAS-89 benchmark circuits for test pattern generation. The test patterns are obtained after enabling compaction option of ATALANTA.

These circuits are generated by removing the flip-flops from the ISCAS-89 original circuits, and by making the inputs to the flip-flops as pseudo-primary outputs and outputs of the flip-flops as pseudo primary inputs to the combinational part. Hope is a parallel fault simulation tool. In our experiment we have used this tool for incremental fault simulation.

For better understanding we illustrate the steps of the experiment on ISCAS–89 benchmark circuit s27 in Table 5.1 and Table 5.2 in detail. ISCAS-89 benchmark circuit s27 has 4 inputs, 1 output, 3 flip-flops and 10 gates. There are 32 faults. The test patterns generated by ATALANTA is given in Table 5.1. Test sequence generated by our approach is given in Table 5.2.

Pattern No.	PI	Scan In	PO	Scan Out	Faults Detected
1	0101	000	1	001	13
2	1000	010	1	100	7
3	0110	110	1	000	2
4	0101	010	0	011	5
5	1000	001	1	101	1
6	0010	010	0	010	1
7	1001	010	0	010	3

Table 5.1: Test vectors for S27 generated by ATALANTA

In table 5.1 the column 2 indicates the primary input value of the corresponding test pattern. The column 3 labeled Scan In represents the pseudo-primary input that needs to be kept in flip-flops through shift in/out through linear scan chain. The column 3, represents the primary output whereas the column 4 labeled as Scan Out represents the pseudo-primary output and the last column illustrates the number of faults detected by that particular test pattern. Here me need to observe the output for 7 times.

On the other hand, the experimental result (experiment is carried out on ISCAS -89 benchmark circuit S27) guided by our approach is illustrated in Table 5.2. The first column of Table 5.2 gives the mode of operation. According to our approach there are two modes of operation, STTMCR (applied first) and LSTMCR (applied when STTMCR is unable to detect any new fault). Here are 3 new columns (1, 5 and 8) labeled Operating Mode, Application Procedure, Activity of PPO (pseudo primary output). Operating mode (Column 1) is explained above. There are 3 categories of application procedure (Column 3). First one is named as “Scan in tree” inserting pseudo primary input for scan test vector to set flip-flops oriented in tree configuration in STTMCR. The second category “Scan in Linear Chain” is to set flip-flop value with pseudo-primary input for scan vectors in LSTMCR mode. The last category is Circular response where the last pseudo-primary output is used as pseudo-primary input. The 8th column indicates the activity of pseudo-primary output for next clock pulse. When a test vector is able to detect a new fault the pseudo-primary output of last response is

used as pseudo-primary input of next clock pulse. Otherwise we scan out the output for observation.

Operating Mode	Pattern No	PI	PPI	Application Procedure	PO	PPO	Activity of PPO	Faults Detected
Scan Tree Test Mode (STTMCR)	1	0101	000	Scan in tree	1	001	PPI of next Vector	13
	2	1000	001	Circular Response	1	101	-do-	3
	3	0010	101	-do-	1	000	-do-	2
	4	1000	000	-do-	1	100	-do-	3
	5	1001	100	-do-	1	100	Scan Out	1
	6	1001	000	Scan in tree	0	010	PPI of next Vector	6
	7	1000	010	Circular Response	1	100	Scan Out	1
	8	0101	011	Scan in tree	0	011	PPI of next Vec.	2
	9	0010	011	Circular Response	0	010	Scan Out	1
Linear Scan Test Mode (LSTMCR)	10	0110	011	Scan in Linear chain	0	010	Scan Out	1

Table 5.2: Test vectors and test sequence for S27 generated by our approach

Circuit Name	Number of flip-flops (*f*)	Number of Test vectors (y)	Total faults	Fault coverage	# scan shifts $(y * f)$
S298	14	31	308	100%	434
S344	15	24	342	100%	360
S386	6	71	384	100%	426
S953	29	95	1079	100%	2755
S1196	18	139	1242	100%	2502
S1238	18	150	1355	95%	2700
S1423	74	62	1515	99.076%	4588
S1488	6	127	1486	100%	762
S1494	6	126	1506	99.203%	756
S15850.1	534	443	11725	96.682%	236562
S35932	1728	65	39094	89.804%	112320

Table 5.3: Results of ATALANTA with the specification of benchmark Circuit ISCAS-89

Circuit Name	Number of flip-flops (*f*)	Depth of the tree $\lceil \log(f) \rceil$	Number of Scan Test vectors (x)	Number of Circular Test vectors	Total faults	Fault coverage	% reduction in the num. of scan vec.(z)
S298	14	4	25	18	308	100%	19
S344	15	4	17	16	342	100%	29
S386	6	3	57	21	384	100%	20
S953	29	5	87	31	1079	100%	9
S1196	18	5	67	103	1242	100%	59
S1238	18	5	60	57	1355	95%	60
S1423	74	7	49	56	1515	99.076%	21
S1488	6	3	91	48	1486	100%	29
S1494	6	3	67	77	1506	99.203%	47
S15850.1	534	10	384	160	11725	96.682%	14
S35932	1728	11	23	51	39094	89.804%	65

Table 5.4: Results of our approach with the specification of benchmark Circuit ISCAS-89

Circuit name	Scan Tree Mode (STTMCR)			Linear Scan Mode (LSTMCR)			# scan shifts (a)	% reduction in no of clock pulse in test mode due to shift (b)
	SV1	CV	FC	SV2	CV	FC		
S298	5	18	83.44%	20	0	100%	300	31
S344	7	16	93.56%	10	0	100%	178	51
S386	11	21	71.09%	46	0	100%	309	28
S953	15	31	64%	72	0	100%	1947	29
S1196	67	103	100%	-	-	100%	335	87
S1238	59	57	95%	1	0	95%	313	88
S1423	9	56	91.28%	40	0	99.076%	3023	34
S1488	16	48	80%	75	0	100%	498	35
S1494	12	77	87%	55	0	99.203%	366	52
S15850.1	34	160	81.86%	350	0	96.682%	187240	21
S35932	8	51	89.809%	15	0	89.809%	26008	77

Table 5.5: Results of Our approach in detail with the specification of benchmark Circuit ISCAS-89

SV- Scan Vectors, CV – Circular Vectors, FC – Fault Coverage,

Experiments are carried out on several ISCAS-89 scan benchmark circuits specified in table 5.3. The improvement using proposed approach over ATALANTA is tabulated in Table 5.4 and 5.5. The improvement is in on the number of scan test vectors and the reduced test application time. In Table 5.3 the last column indicates the number of clock pulses due to shift in testing mode. The last column of Table 5.4 shows the percentile reduction of number of scan vectors and here z is evaluated as $z = (y - x)/y * 100$.

Here the 1st (SV1), 2nd (CV) and 3rd (FC) sub columns of 2nd column (named as Scan tree mode (STTMCR)) represents Scan vectors, Circular vectors and fault coverage in Scan tree test mode. Here the pseudoprimary input of scan vectors are pushed in the scan tree in $log\lceil(no\ of\ flip\text{-}flops)\rceil$ unit of time that is the main advantage of our approach. FC indicates the fault coverage in Scan Tree Mode (STTMCR).

The 1st (SV2), 2nd (CV) and 3rd (FC) sub columns of 3rd column (named as Linear Scan mode (LSTMCR)) represents Scan vectors, Circular vectors in Linear Scan Test Mode and FC is the fault coverage after this mode. Here the number of scan vectors is more compared to Scan tree mode because here the hard to detect faults are dealt with, so each scan vector has very poor fault coverage. Here the CV column entries are all zeros because hard to detect faults are not easy to be detected by circulating the pseudo primary output to next clock pseudoprimary input. The last column FC detects the fault coverage after two modes of operation. Here the 4th column named as (# scan shifts (a)) show the no of clock pulse needed due to shift and here $a = (SV1 * \lceil \log(f) \rceil) + (SV2 * f)$. The last column represents (% reduction in no of clock pulse due to shift (b)) by the proposed approach over ATALANTA and b is calculated as $b = (((a - y * f) / (y * f)) * 100)$. The experiential results show that the proposed approach is advantageous.

Chapter 6

Conclusion and Scope of future work

Conclusion

A new circuit independent and test set independent hybrid test architecture is described here and empirically evaluated, which shows improvement in test application time and power/energy consumption reduction. The technique uses circulation of responses to be used as tests, which drastically reduces total number of shift operations.

The architecture provides an improved controllability and observability. This test architecture can be implemented for BIST very easily. The proposed method will be useful in transition testing, as circulating tests, being applied in non-scan mode, can be fed at speed, and the corresponding errors can be accumulated and observed in the scan out mode. Further, the scheme helps in reducing test and response data, because, the number of vectors to be scanned in from the tester as well as the response vector to be scanned out are reduced significantly.

Although non-scan test mode is being used in part, no sequential ATPG is required. Only a combinational ATPG is required to generate initial set of test vectors.

Scope of future work

The experimental result shows that we are in the right track. Though we may increase the performance of the proposed scheme by detecting hard to detect fault and tackling them at first. Our intuition is that, this way will lead to reduce number of scan vector at the cost of circulating vectors, which would be more desirable. Currently this is under implementation.

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